ADSP-21061L SHARC®
Preliminary Data Sheet

SUMMARY

- **High-Performance Signal Computer for Speech, Audio, Graphics, Control, and Imaging Applications**
- **Super Harvard ARchitecture Computer (SHARC) Four Independent Buses for Dual Data, Instructions, and I/O**
- **32-Bit IEEE Floating-Point Computation Units Multiplier, ALU, and Shifter**
- **1 Megabit On-Chip SRAM Memory and Integrated I/O Peripherals - A Complete System-On-A-Chip**
- **Integrated Multiprocessing Features**

KEY FEATURES

- 40 MIPS, 25 ns Instruction Rate, Single-Cycle Instruction Execution
- 120 MFLOPS Peak, 80 MFLOPS Sustained Performance
- Dual Data Address Generators with Modulo and Bit-Reverse Addressing
- Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
- IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation
- 240-Lead PQFP Package
- Pin-Compatible with ADSP-21060 (4 Mbit), ADSP-21062 (2 MBit), and ADSP-21061 (5V 1Mbit)
- 3.3 Volt Operation

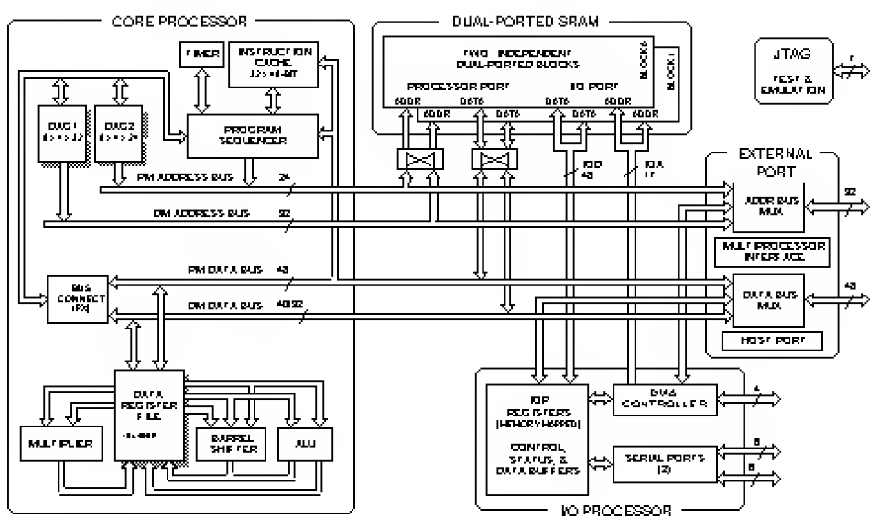


Figure 1 ADSP-21061L Functional Block Diagram

FEATURES (continued)

Flexible Data Formats & 40-Bit Extended Precision:

- 32-Bit Single-Precision & 40-Bit Extended-Precision IEEE Floating-Point Data Formats
- 32-Bit Fixed-Point Data Format, Integer & Fractional, with 80-Bit Accumulators

Parallel Computations:

- Single-Cycle Multiply & ALU Operations in Parallel with Dual Memory Read/Writes & Instruction Fetch
- Multiply with Add & Subtract for Accelerated FFT Butterfly Computation
- 1024-Point Complex FFT Benchmark: 0.46 msec (18,221 cycles)

1 Megabit Configurable On-Chip SRAM:

- Dual-Ported for Independent Access by Core Processor and DMA
- Configurable as 32K Words Data Memory (32-Bit), 16K Words Program Memory (48-Bit), or Combinations of Both Up To 1 Mbit

Off-Chip Memory Interfacing:

- 4 Gigawords Addressable (32-bit Address)
- Programmable Wait State Generation, Page-Mode DRAM Support

DMA Controller:

- 6 DMA Channels
- Background DMA Transfers at 40 MHz, in Parallel with Full-Speed Processor Execution
- Performs Transfers Between ADSP-21061L Internal Memory and External Memory, External Peripherals, Host Processor, or Serial Ports

Host Processor Interface:

- Efficient Interface to 16- & 32-Bit Microprocessors
- Host can Directly Read/Write ADSP-21061L Internal Memory message, and IO registers

Multiprocessing:

- Glueless Connection for Scalable DSP Multiprocessing Architecture
- Distributed On-Chip Bus Arbitration for Parallel Bus Connect of Up To 6 ADSP-21061Ls Plus Host
- 240 Mbytes/s Transfer Rate Over Parallel Bus

Serial Ports:

- Two 40 Mbit/s Synchronous Serial Ports
- Independent Transmit & Receive Functions
- 3- to 32-Bit Data Word Width
- µ-Law/A-Law Hardware Companding
- TDM Multichannel Mode
- Multichannel Signaling Protocol

GENERAL DESCRIPTION

The ADSP-21061L is a member of the powerful SHARC family of floating point processors. The SHARC—Super Harvard ARchitecture Computer—are signal processing microcomputers that offer new capabilities and levels of integration and performance. The ADSP-21061L is a 32-bit processor optimized for high performance DSP applications. The ADSP-21061L combines the ADSP-21000 DSP core with a dual-ported on-chip SRAM and an I/O processor with a dedicated I/O bus to form a complete system-in-a-chip.

Fabricated in a high-speed, low-power CMOS process, the ADSP-21061L has a 25 ns instruction cycle time operating at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 1 shows performance benchmarks for the ADSP-21061L.

The ADSP-21061L SHARC combines a high-performance floating-point DSP core with integrated, on-chip system features including a 1 Mbit SRAM memory, host processor interface, DMA controller, serial ports, and parallel bus connectivity for glueless DSP multiprocessing.

Figure 1 shows a block diagram of the ADSP-21061L, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with
- A Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Interval Timer
- On-Chip SRAM
- External Port for Interfacing to Off-Chip Memory & Peripherals
- Host Port & Multiprocessor Interface
- DMA Controller
- Serial Ports
- JTAG Test Access Port

Figure 2 shows a typical single-processor system.

A multiprocessor system is shown in Figure 3.

Table 1 ADSP-21061L Benchmarks (@ 40 MHz)

1024-Pt. Complex FFT (Radix 4, with digit reverse)	**0.46 msec**	**18,221 cycles**
FIR Filter (per tap)	**25 ns**	**1 cycle**
IIR Filter (per biquad)	**100 ns**	**4 cycles**
Divide (y/x)	**150 ns**	**6 cycles**
Inverse Square Root (1/Ðx)	**225 ns**	**9 cycles**
DMA Transfer Rate	**240 Mbyte/s**	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-21061L includes the following architectural features of the ADSP-21000 Family core. The ADSP-21061L is code and function compatible with the ADSP-21060/62 and the ADSP-21020.

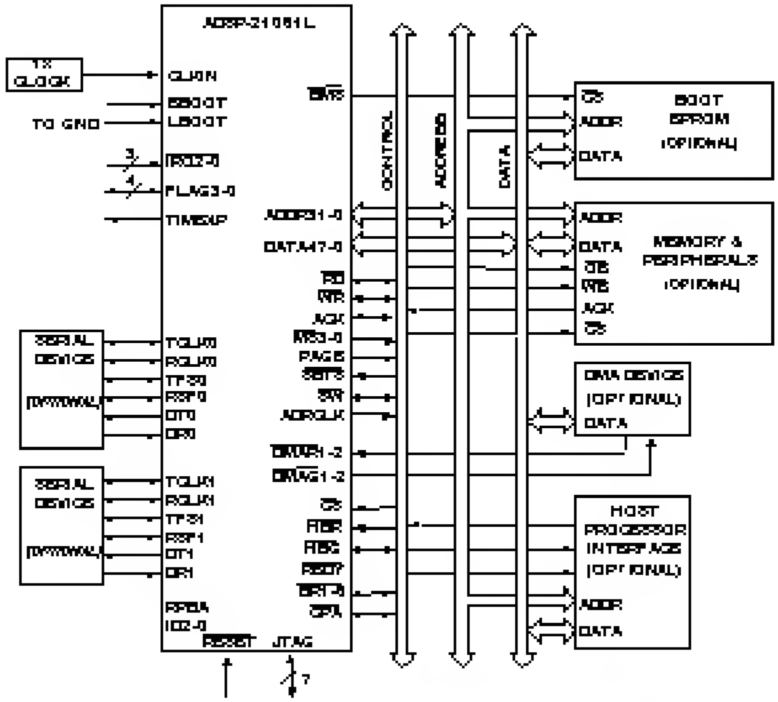


Figure 2 ADSP-21061L System

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction & Two Operands

The ADSP-21061L features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21061L includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21061L's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21061L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21061L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21061L FEATURES

Augmenting the ADSP-21000 family core, the ADSP-21061L adds the following architectural features:

Dual-Ported On-Chip Memory

The ADSP-21061L contains 1 megabit of on-chip SRAM, organized as two banks of 0.5 Mbits each. Each bank has eight 16-bit columns with 4K 16-bit words per column. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21061L Memory Map).

On the ADSP-21061L, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words for 16-bit data, 16K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 1 megabits. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

A 16-bit floating-point storage format is supported which effectively doubles the amount of data that may be stored on chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-

chip, via the ADSP-21061L's external port.

Off-Chip Memory & Peripherals Interface

The ADSP-21061L's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-21061L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus. The on-chip SuperHarvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21061L provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

Host Processor Interface

The ADSP-21061L's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-21061L's external port and is memory-mapped into the unified address space. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21061L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-21061L, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DMA Controller

The ADSP-21061L's on-chip DMA controller allows zero-overhead, non-intrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21061L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21061L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16, 32, or 48-bit words is performed during DMA transfers.

Six channels of DMA are available on the ADSP-21061L—four via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21061Ls, memory or I/O transfers). Programs can be downloaded to the ADSP-21061L using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines (DMAR1-2, DMAG1-2). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports

The ADSP-21061L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial port also include keyword and keymask features to enhance interprocessor communication.

Multiprocessing

The ADSP-21061L offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of each ADSP-21061L's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21061Ls and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240 Mbytes/sec over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21061Ls and can be used to implement reflective semaphores.

Program Booting

The internal memory of the ADSP-21061L can be booted at system powerup from either an 8-bit EPROM or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (Boot Memory Select), EBOOT (EPROM Boot), and LBOOT (Host Boot) pins. 32-bit and 16-bit host processors can be used for booting. See the $\overline{\text{BMS}}$ pin in the "Pin Descriptions" section of this data sheet.

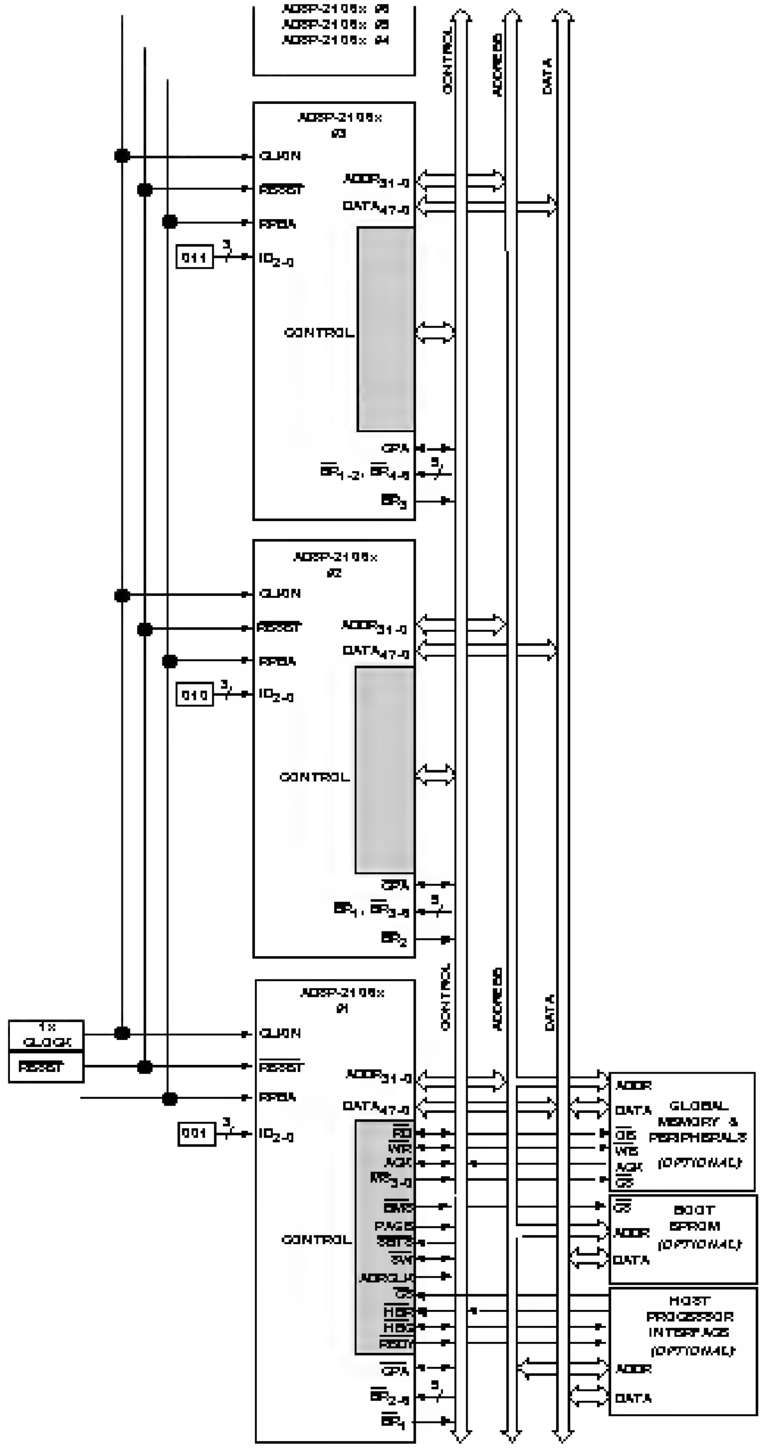


Figure 3 Multiprocessing System

ADSP-21061L MEMORY MAP

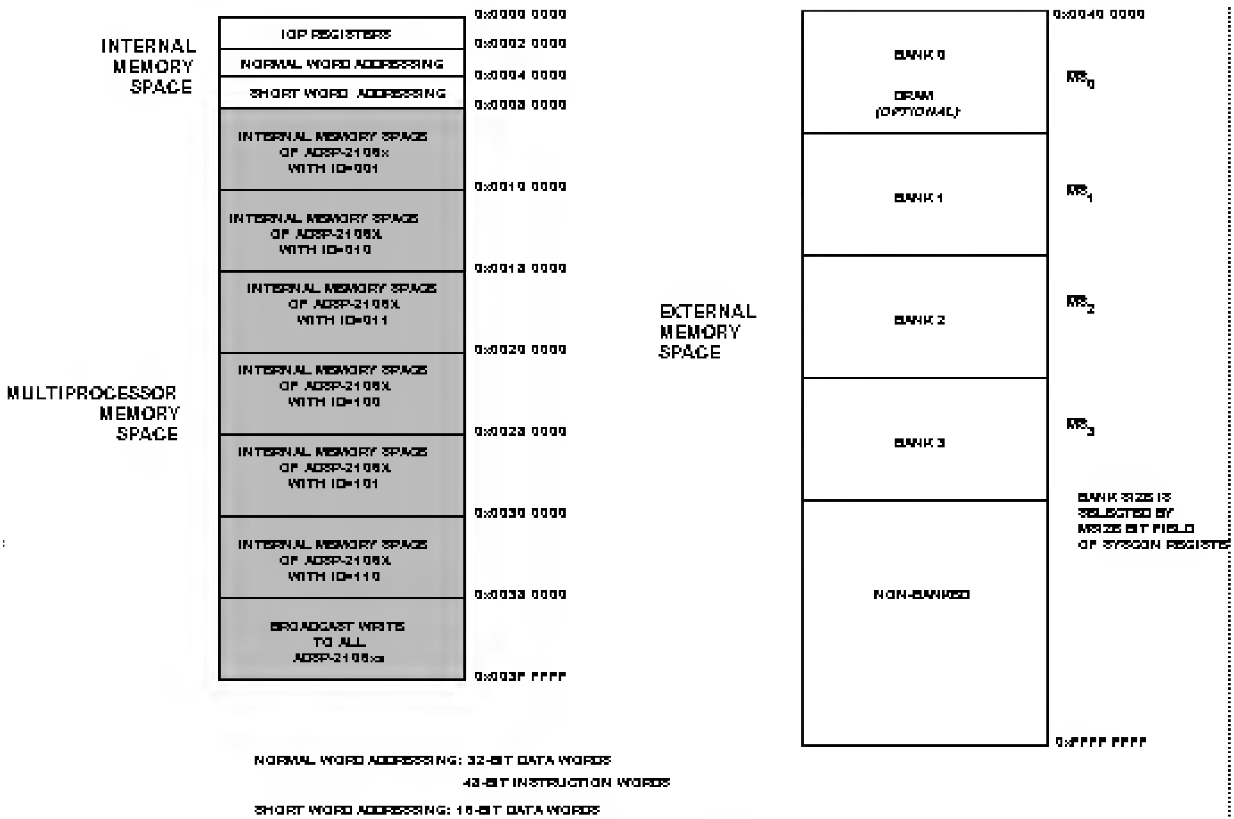


Figure 4 ADSP-21061L Memory Map

Porting Code from ADSP-21060 or ADSP-21062 to the ADSP-21061L

The ADSP-21061L is pin compatible with the ADSP-21060/61/62 processors.

The ADSP-21061L pins that correspond to the Link Port pins of the ADSP-21060/62 are no-connects

The ADSP-21061L is object code compatible with the ADSP-21060/62 except for the following functional changes:

> The ADSP-21061L memory is organized into two blocks with eight columns that are 4K deep per block. The ADSP-21060/62 memory has 16 columns per block.
>
> Link Port functions are not available.
>
> Handshake external port DMA pins $\overline{\text{DMAR2}}$ and $\overline{\text{DMAG2}}$ are assigned to external port DMA Channel 6 instead of channel 8.
>
> 2-D DMA capability of the SPORT is not available.
>
> The modify registers in SPORT DMA are not available.

On the ADSP-21061L, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into block that alias into Block 1. This allows any code or data stored in Block 1 of the ADSP-21062 to retain the same addresses

on the ADSP-21061L–these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061L, use only the first eight columns of each memory bank. Limit your application to 8K of instructions or up to 16K of data in each bank of the ADSP-21062, or any combinations of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

The ADSP-21061L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator, EZ-Kit Lite, and development software. The SHARC EZ-Kit Lite (ADDS-2106x-EZ-LITE) is a complete low cost package for DSP evaluation and prototyping. The EZ-Kit Lite contains an evaluation board with an ADSP-21061 (5V) processor and provides a serial connection to your PC. The EZ-Kit Lite also includes an optimizing compiler, assembler, instruction level simulator, run-time libraries, diagnostic utilities, and a complete set of example programs.

The same EZ-ICE hardware that you use for the ADSP-21060/62, also fully emulates the ADSP-21061L, with the exception of displaying and modifying the two new SPORTs registers. The emulator will not display these two registers, but your code can use them.

Analog Devices ADSP-21000 Family Development Software includes an easy to use Assembler based on an algebraic syntax, Assembly Library/Librarian, Linker, instruction—level Simulator, an ANSI C optimizing Compiler, the CBug™ C Source—Level Debugger, and a C Runtime Library including DSP and mathematical functions. The Optimizing Compiler includes Numerical C extensions based on the work of the ANSI Numerical C Extensions Group. Numerical C provides extensions to the C language for array selections, vector math operations, complex data types, circular pointers, and variably dimensioned arrays. The ADSP-21000 Family Development Software is available for both the PC and Sun platforms.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21061L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Non-intrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

Further details and ordering information are available in the ADSP-21000 Family Hardware & Software Development Tools data sheet (ADDS-210xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs' and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

Additional Information

This preliminary data sheet provides a general overview of the ADSP-21061L architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the ADSP-2106x SHARC User's Manual, Second Edition.

PIN DESCRIPTIONS

ADSP-21061L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{TRST}$).

Unused inputs should be tied or pulled to IVDD or IGND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{SW}$, and inputs that have internal pullup or pulldown resistors ($\overline{CPA}$, ACK, DTx, DRx, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating.These pins have a logic-level hold circuit that prevents the input from floating internally.

I=Input	S=Synchronous	P=Power Supply	(o/d)=Open Drain
O=Output	A=Asynchronous	G=Ground	(a/d)=Active Drive

T=Three-state (when $\overline{SBTS}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address**. The ADSP-21061L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-21061L inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data**. The ADSP-21061L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 47-16. 40-bit extended-precision floating-point data is transferred over bits 47-8 of the bus. 16-bit short word data is transferred over bits 31-16 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	**Memory Select Lines**. These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-21061L's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessor system the $\overline{MS}_{3-0}$ lines are output by the bus master.

Pin	Type	Function
$\overline{RD}$	I/O/T	**Memory Read Strobe**. This pin is asserted (low) when the ADSP-21061L reads from external memory devices or from the internal memory of other ADSP-21061Ls. External devices (including other ADSP-21061Ls) must assert $\overline{RD}$ to read from the ADSP-21061L's internal memory. In a multiprocessor system $\overline{RD}$ is output by the bus master and is input by all other ADSP-21061Ls.
$\overline{WR}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-21061L writes to external memory devices or to the internal memory of other ADSP-21061Ls. External devices must assert $\overline{WR}$ to write to the ADSP-21061L's internal memory. In a multi-processor system $\overline{WR}$ is output by the bus master and is input by all other ADSP-21061Ls.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-21061L asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-21061L's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessor system PAGE is output by the bus master.
ADRCLK	O/T	**Address Clock** for synchronous external memories. Addresses on ADDR31-0 are valid before the rising edge of ADRCLK. In a multiprocessing system ADRCLK is output by the bus master.
$\overline{SW}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-21061Ls). The ADSP-21061L asserts $\overline{SW}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{WR}$ is not later asserted (e.g. in a conditional write instruction). In a multiprocessor system, $\overline{SW}$ is output by the bus master and is input by all other ADSP-21061Ls to determine if the multiprocessor memory access is a read or write. $\overline{SW}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-21061L(s).
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21061L deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessor system, a slave ADSP-21061L deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.

Pin	Type	Function
$\overline{SBTS}$	I/S	**Suspend Bus Three-state.** External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high-impedance state for the following cycle. If the ADSP-21061L attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from PAGE faults or host processor/ADSP-21061L deadlock.
$\overline{IRQ}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
$FLAG_{3-0}$	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21061L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21061L that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21061L places the address, data, select, and strobe lines in a high-impedance state. $\overline{HBR}$ has priority over all ADSP-21061L bus requests ($\overline{BR}_{6-1}$) in a multiprocessor system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-21061L until $\overline{HBR}$ is released. In a multiprocessor system, $\overline{HBG}$ is output by the ADSP-21061L bus master and is monitored by all others.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21061L.
REDY (o/d)	O	**Host Bus Acknowledge.** The ADSP-21061L deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (o/d) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (a/d). REDY will only be output if the CS and HBR inputs are asserted.
DMAR1	I/A	**DMA Request 1** (DMA Channel 7).
DMAR2	I/A	**DMA Request 2** (DMA Channel 6).
DMAG1	O/T	**DMA Grant 1** (DMA Channel 7).
DMAG2	O/T	**DMA Grant 2** (DMA Channel 6).

Pin	Type	Function
$\overline{BR}_{6-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21061Ls to arbitrate for bus mastership. An ADSP-21061L only drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21061Ls, the unused $\overline{BR}$x pins should be tied high; the processor's own $\overline{BR}$x line must not be tied high or low because it is an output.
ID_{2-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$ – $\overline{BR}_6$) is used by ADSP-21061L. ID=001 corresponds to $\overline{BR}_1$, ID=010 corresponds to $\overline{BR}_2$, etc. ID=000 in single-processor systems. These lines are a system configuration selection which should be hard-wired or only changed at reset.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21061L. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21061L.
$\overline{CPA}$ (o/d)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21061L bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to all ADSP-21061Ls in the system. The $\overline{CPA}$ pin has an internal 5 Kohm pullup resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DTx	O	**Data Transmit** (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pullup resistor.
DRx	I	**Data Receive** (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pullup resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pullup resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pullup resistor.
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-21061L is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{BMS}$ inputs determine booting mode. See table below. This signal is a system configuration selection which should be hard-wired.
LBOOT	I	**Link Boot** – Must be tied to GND.

Pin	Type	Function
$\overline{BMS}$	I/O/T*	**Boot Memory Select.** Output: Used as chip select for boot EPROM devices (when EBOOT=1, LBOOT=0). In a multiprocessor system, $\overline{BMS}$ is output by the bus master. Input: When low, indicates that no booting will occur and that ADSP-21061L will begin executing instructions from external memory. See table below. This input is a system configuration selection which should be hard-wired. * Three statable only in EPROM boot mode (when BMS is an output).

EBOOT	LBOOT	BMS	Booting Mode
1	0	output	EPROM (connect $\overline{BMS}$ to EPROM chip select)
0	0	1 (input)	Host processor
0	0	0 (input)	No booting. Processor executes from external memory.

Pin	Type	Function
CLKIN	I	**Clock In.** External clock input to the ADSP-21061L. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{RESET}$	I/A	**Processor Reset.** Resets the ADSP-21061L to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pullup resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pullup resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{TRST}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21061L. $\overline{TRST}$ has a 20 kΩ internal pullup resistor.
$\overline{EMU}$	O	**Emulation Status.** Must be connected to the ADSP-21061L EZ-ICE target board connector only.
ICSA	O	Reserved, leave unconnected.
V_{DD}	P	**Power Supply;** nominally +3.3V dc. (30 pins)
GND	G	**Power Supply Return**. (30 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-21061L EZ-ICE emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21061L to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-21061L's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$, and GND signals be made accessible on the target system via a 14-pin connector (a pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you, intend to use the ADSP-21061L EZ-ICE. The length of the traces between the connector and the ADSP-21061L's JTAG pins should be as short as possible.

The 14-pin, 2-row pin strip header is keyed at the pin 3 location—you must remove pin 3 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 x 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

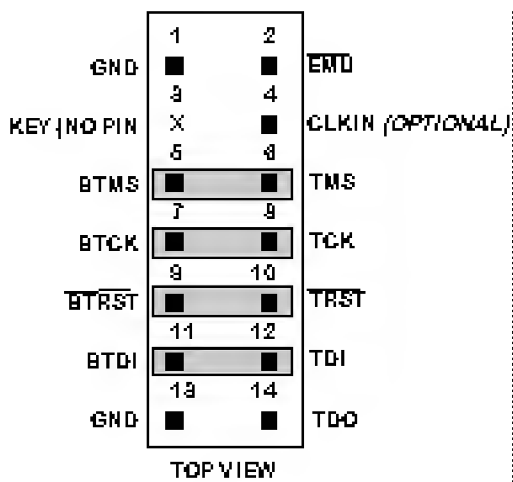


Figure 5 Target Board Connector for ADSP-21061L EZ-ICE

The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the BXXX pins and the XXX pins. If you are not going to use the test access port for board testing, tie BTRST to GND and tie or pullup BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-21061L. None of the BXXX pins (pins 5, 7, 9, 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as follows:

Signal	Termination
TMS	Driven through 82Ω resistor (16 mA /-3.2mA driver)
TCK	Driven AT 10 MHz through 82Ω resistor (16 mA /-3.2mA driver)
$\overline{\text{TRST}}$	Driven through 82Ω resistor (16 mA /-3.2mA driver) (pulled up by on-chip 20kΩ resistor)
TDI	Driven by 82Ω resistor (16 mA /-3.2mA driver)
TDO	One TTL load, 92Ω thevenin termination (160/220)
CLKIN	One TTL load, 92Ω thevenin termination (160/220)
$\overline{\text{EMU}}$	4.7 kΩ pullup resistor, one TTL load (open-drain output from ADSP-21061Ls)

* $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, $\overline{\text{TRST}}$ is driven high.

Figure 7 shows JTAG scan path connections for systems that contain multiple ADSP-21061L processors.

Connecting CLKIN to pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-21061Ls in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21061L processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one cycle between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-21061Ls (more than eight) in your system, then treat them as a clock tree" using multiple drivers to minimize skew. (See Figure 6 "JTAG Clock Tree" on the following page and Clock Distribution" in the "High Frequency Design Considerations" section of the ADSP-2106x User's Manual, Second Edition).

If synchronous multiprocessor operations are not needed (i.e. CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$ and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For Complete information on the SHARC EZ-ICE, see the ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference.

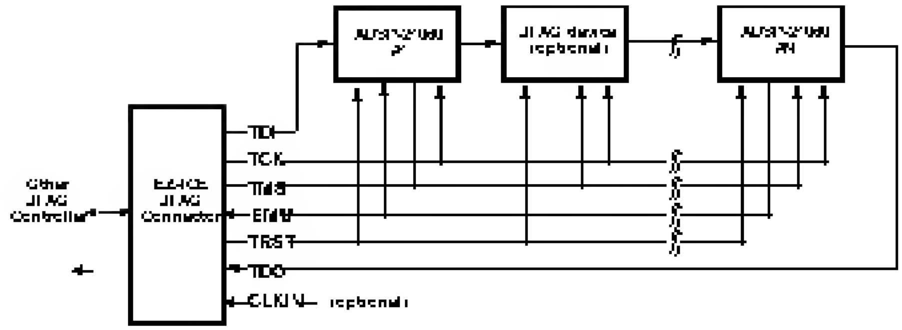


Figure 6 JTAG Clocktree for Multiple ADSP-2106x Systems

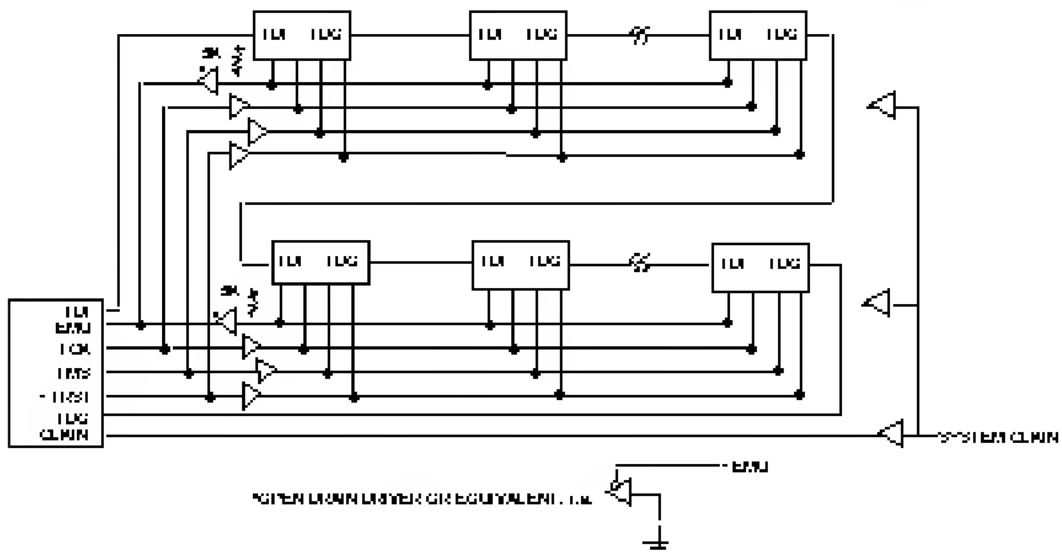


Figure 7 JTAG Scan Path Connections for Multiple ADSP-2106x Systems

PRELIMINARY SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	Max	Unit
V_{DD}	Supply Voltage	3.15	3.45	V
T_{CASE}	Case Operating Temperature	0	+85	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH1}	High Level Input Voltage[1]	@V_{DD} = max	2.0	V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	@V_{DD} = max	2.2	V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	@V_{DD} = min	-0.5	0.8	V
V_{OH}	High Level Output Voltage[3]	@V_{DD} = min, I_{OH} = – 2.0 mA[12]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@V_{DD} = min, I_{OL} = 4.0 mA[12]		0.4	V
I_{IH}	High Level Input Current[4]	@V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[4]	@V_{DD} = max, V_{IN} = 0V		10	µA
I_{ILP}	Low Level Input Current[5]	@V_{DD} = max, V_{IN} = 0V		150	µA
I_{OZH}	Three-State Leakage Current [6, 7,13 ,15]	@V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@V_{DD} = max, V_{IN} = 0V		10	µA
I_{OZHP}	Three-State Leakage Current[11]	@V_{DD} = max, V_{IN} = V_{DD} max		350	
I_{OZLC}	Three-State Leakage Current[13]	@V_{DD} = max, V_{IN} = 0V		1.5	mA
I_{OZLA}	Three-State Leakage Current[14]	@V_{DD} = max, V_{IN} = 0V		350	µA
I_{OZLAR}	Three-State Leakage Current[15]	@V_{DD} = max, V_{IN} = 1.5V		4.2	mA
I_{OZLS}	Three-State Leakage Current[7]	@V_{DD} = max, V_{IN} = 0V		150	µA
I_{DDINI}	Supply Current (Internal)[8]	t_{CK} = 25 ns, V_{DD} = max,		600	mA
I_{DDIN2}	Supply Current (Internal)[16]	t_{CK} = 25 ns, V_{DD} = max,		460	mA
$I_{DDIDLE16}$	Supply Current (Idle16)[17]	V_{DD} = max		50	mA
I_{DDIDLE}	Supply Current (Idle)[9]	V_{DD} = max		200	mA
C_{IN}	Input Capacitance[10, 11]	f_{IN} = 1 MHz, T_{CASE} = 25 °C, V_{IN} = 2.5V		4.7	pF

NOTES

1 Applies to input and bidirectional pins: DATA47-0, ADDR31-0, EBOOT, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}$2-0, FLAG3-0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, HBR, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

2 Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

3 Applies to output and bidirectional pins: DATA47-0, ADDR31-0, MS3-0, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA

4 Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2K¾ during reset in a multiprocessor system, when ID2-0=001 and another ADSP-2106x is not requesting bus mastership.)

5 Applies to input pins with internal pullups: DR0, DR1, $\overline{TRST}$, TMS, TDI

6 Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, TDO, and $\overline{EMU}$ (Note that ACK is pulled up internally with 2KΩ during reset in a multiprocessor system, when ID2-0=001 and another ADSP-21061L is not requesting bus mastership).

7 Applies to three-statable pins with internal pullups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1

8 Applies to V_{DD} pins. See "Power Dissipation" for calculation of external supply current (at EVDD pins) and total supply current. Conditions of operation: Executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from each internal memory block, and one DMA transfer occurring from/to internal memory at T_{CK} = 30ns, I_{DDIN} = 750 max.

9 Applies to V_{DD} pins. Idle denotes ADSP-21061L state during execution of IDLE instruction.

10 Applies to all signal pins.

11 Guaranteed but not tested.

12 See "Output Drive Currents" for typical drive current capabilities.

13 Applies to $\overline{CPA}$ pin.

14 Applies to ACK pin when keeper latch enabled. (Note that ACK is pulled up internally with a 2KΩ during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-21061L is not requesting bus mastership).

15 Applies to ACK pin when pulled up.

16 Applies to V_{DD} pins. See "Power Dissipation" for calculation of external supply current (at EVDD pins) and total supply current. Conditions of operation: Executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from each internal memory block, at T_{CK} = 30ns, I_{DDIN2} = 540 max.

17 Applies to V_{DD} pins. Idle 16 denotes ADSP-21061L state during execution of IDLE16 instruction.

Absolute Maximum Ratings

Supply Voltage	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} +0.5 V
Load Capacitance	200 pF
Junction Temperature Under Bias	130°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (5 seconds)	+280°C

Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Sensitivity

The ADSP-2106x processors are ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2106x processors include proprietary ESD protection circuitry to dissipate high energy discharges. Per method 3015 of MIL-STD-883, the ADSP-21061L processor has been classified as a Class TBD device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.

PRELIMINARY TIMING SPECIFICATIONS

GENERAL NOTES

The following timing specifications are target specifications and are based on device simulations only.

Two speed grades of the ADSP-21061L will be offered, 40 MHz and 33.3 MHz. The specifications shown are based on a CLKIN frequency of 40 MHz (t_{CK}=25 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see "Clock Input" below). DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns:

DT=t_{CK} – 25 ns

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 under "Test Conditions" for voltage reference levels.

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(o/d)=Open Drain
(a/d)=Active Drive

Clock Input

Parameter		40 MHz		33.3 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements:						
t_{CK}	CLKIN Period	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		ns
t_{CKH}	CLKIN Width High	5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4V–2.0V)		3		3	ns

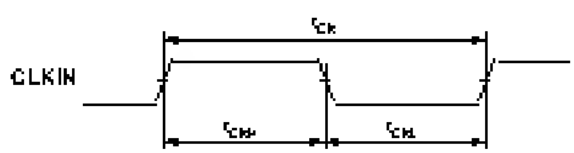


Figure 8 Clock Input

Reset

Parameter		Min	Max	Unit
Timing Requirements:				
t_{WRST}	RESET Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	RESET Setup before CLKIN High [2]	14 + DT/2	t_{CK}	ns

NOTES
1. Applies after the powerup sequence is complete. At powerup, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while RESET is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).
2. Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e. for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

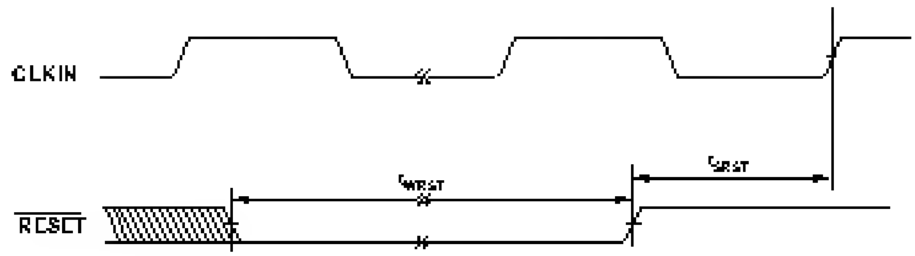


Figure 9 Reset

Interrupts

Parameter:		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ}_{2\text{-}0}$ Setup before CLKIN High 1	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ}_{2\text{-}0}$ Hold before CLKIN High 1		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ}_{2\text{-}0}$ Pulse Width 2	2 + tCK		ns

NOTES
1. Only required for $\overline{IRQ}$x recognition in the following cycle.
2. Applies only if t_{SIR} and t_{HIR} requirements are not met.

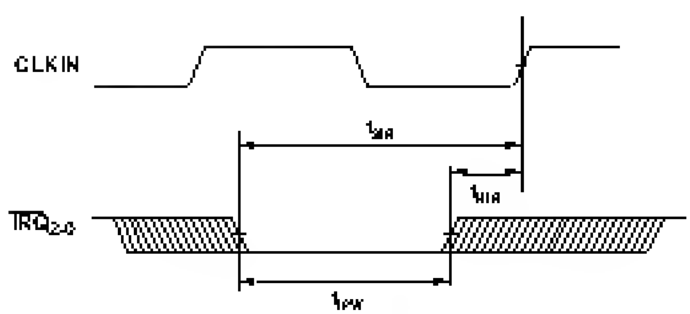


Figure 10 Interrupts

Timer

Parameter		Min	Max	Unit
t_{DTEX}	CLKIN High to TIMEXP		15	ns

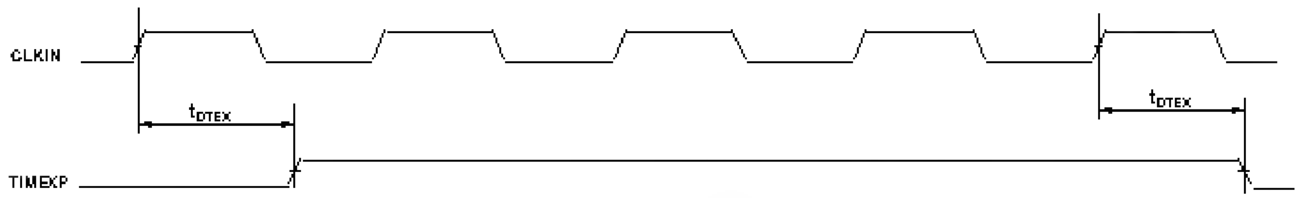


Figure 11 Timer

Flags

Parameter		Min	Max	
Timing Requirements:				
t_{SFI}	FLAG3-0IN Setup before CLKIN High 1	8 + 5DT/16		ns
t_{HFI}	FLAG3-0IN Hold after CLKIN High 1	0 – 5DT/16		ns
t_{DWRFI}	FLAG3-0IN Delay after RD/WR Low 1		5 + 7DT/16	ns
t_{HFIWR}	FLAG3-0IN Hold after RD/WR Deasserted 1	0		ns
Switching Characteristics:				
t_{DFO}	FLAG2-0OUT Delay after CLKIN High		16	ns
t_{HFO}	FLAG2-0OUT Hold after CLKIN High	4		ns
t_{DFOE}	CLKIN High to FLAG2-0OUT Enable	3		ns
t_{DFOD}	CLKIN High to FLAG2-0OUT Disable		14	ns

NOTES
1. Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

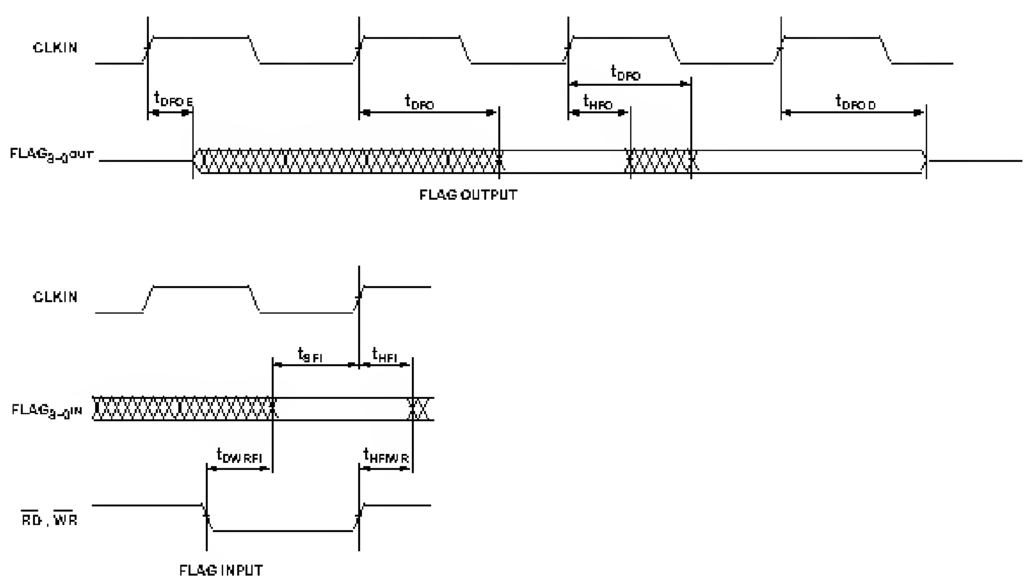


Figure 12 Flags

Memory Read – Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see "Synchronous Read/Write – Bus Master" below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAD}	Address, Selects Delay to Data Valid[1, 4]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12+ 5DT/8 + W	ns
t_{HDA}	Data Hold from Address Selects[2]	0.5		ns
t_{HDRH}	Data Hold from Address, Selects[2]	2.0		ns
t_{DAAK}	ACK Delay from Address[3, 4]		15 + 7DT/8 +W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3]		8 + DT/2 +W	ns
Switching Characteristics:				
t_{DRHA}	Address, Selects hold after $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[4]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup before ADRCLK High[4]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) x t_{CK}
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI=0)
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H=0)

NOTES:

1. Data Delay/Setup: User must meet t_{DAD} or to t_{DRLD} or synchronous specification t_{SSDATI}
2. Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification $t_{HDATI.}$ See "system hold time calculation" under "test conditions" for the calculation of hold times given capacitive and DC loads.
3. ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (low); all three specifications must be met for assertion of ACK (high).
4. The falling edge of MSx, SW, BMS, are referenced.

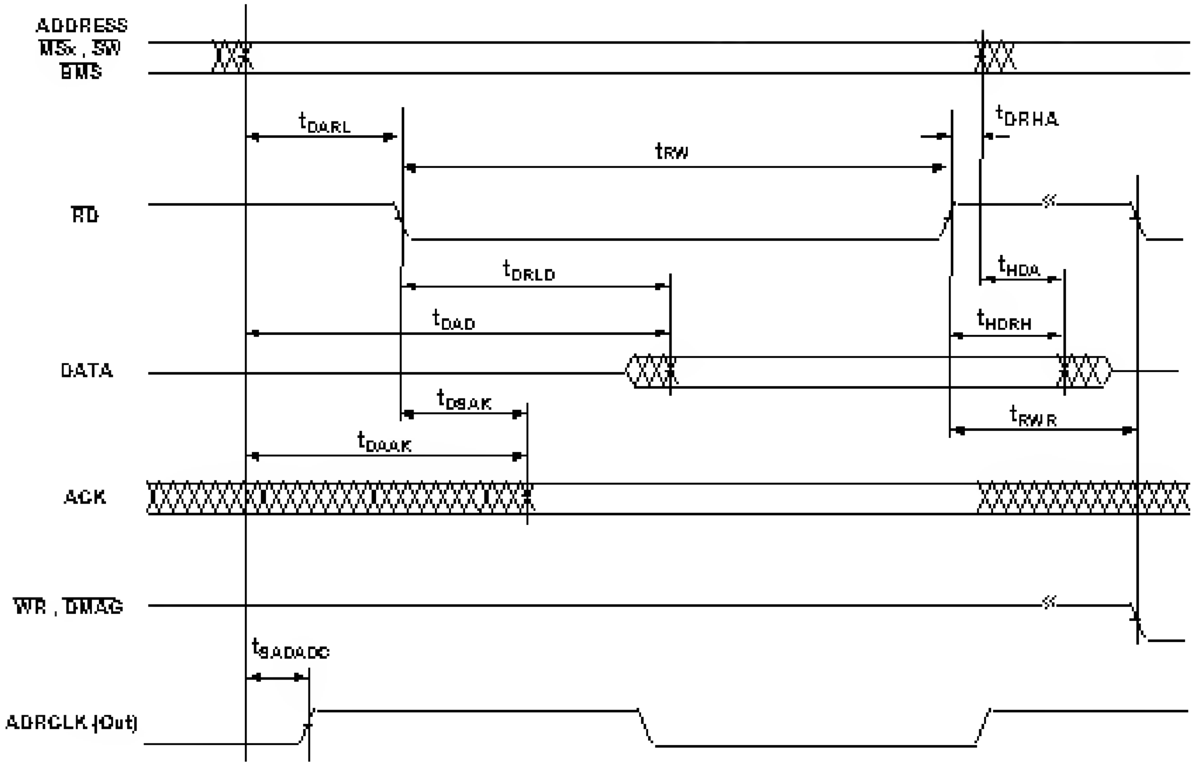


Figure 13 Memory Read – Bus Master

Memory Write – Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see "Synchronous Read/Write – Bus Master" below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1]		15 + 7DT/8 +W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 +W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted	17 + 15DT/16 +W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	13 + DT/2 +W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High	7 + 9DT/16 +W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ Deasserted	1 + DT/16 + H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ Deasserted[2]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–I + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High	0+ DT/4		ns

W = (number of wait states specified in WAIT register) x t_{CK}
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H=0)
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I=0)

NOTES

1. ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (low); all three specifications must be met for assertion of ACK (high).
2. See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and DC loads.

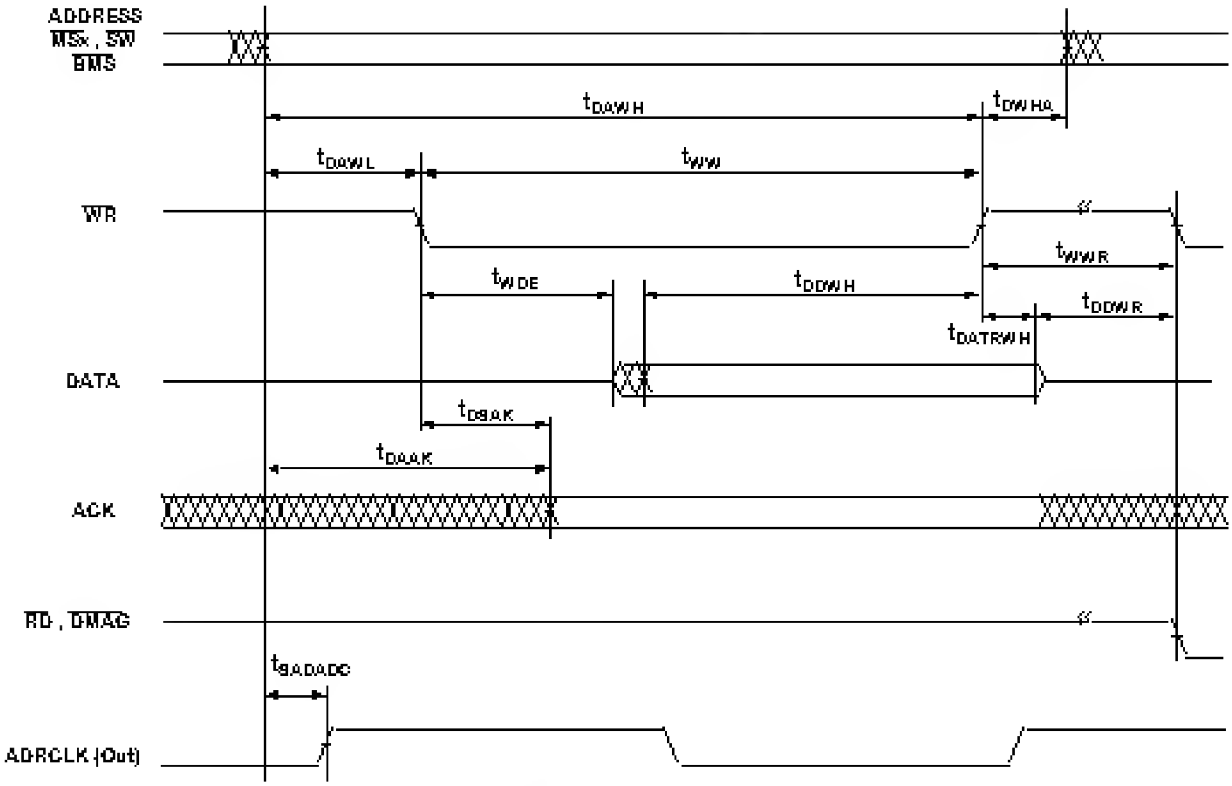


Figure 14 Memory Write – Bus Master

Synchronous Read/Write – Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21061L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see "Memory Read – Bus Master" and "Memory Write – Bus Master").

When accessing a slave ADSP-21061L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see "Synchronous Read/Write – Bus Slave"). The slave ADSP-21061L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup before CLKIN	2 + DT/8		ns
t_{HSDATI}	Data Hold after CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay after Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[2,3]		14 + 7 DT/8 + w	ns
t_{SACKC}	ACK Setup before CLKIN[2]	6.5 + DT/4		ns
t_{HACKI}	ACK Hold after CLKIN	–1 – DT/4		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay after CLKIN[2]		7 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold after CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay after CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay after CLKIN	–1.5 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay after CLKIN	–2.5 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay after CLKIN	8 + DT/4	12 + DT/4	ns
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[1]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay after CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

w = (number of wait states specified in WAIT register) x tCK

NOTES
1. See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and DC loads.
2. Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See "system hold time calculation" under "test conditions" for the calculation of hold times given capacitive and DC loads.
3. ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (low); all three specifications must be met for assertion of ACK (high).

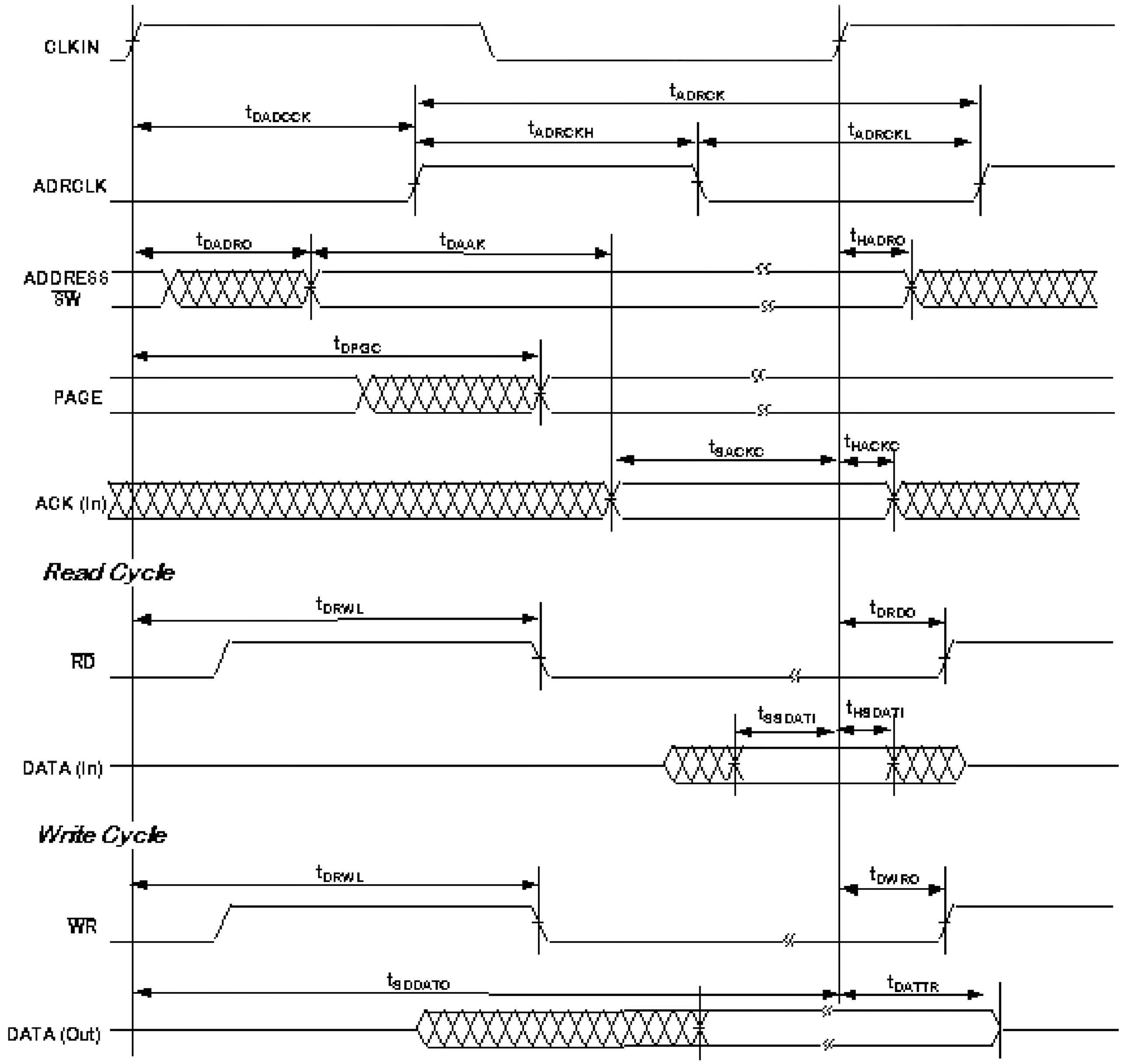


Figure 15 Synchronous Read/Write–Bus Master

Synchronous Read/Write – Bus Slave

Use these specifications for ADSP-21061L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup before CLKIN	14 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold before CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup before CLKIN[1]	8.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold after CLKIN	–4 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	3		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	1		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[2]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay after Address, $\overline{SW}$[3]		8	ns
t_{ACKTR}	ACK Disable after CLKIN[2]	–1 – DT/8	6 – DT/8	ns

NOTES

1. t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.
2. See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and DC loads.
3. t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 9+ 3DT/4. If the address and SW inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with a M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with ACKTR.

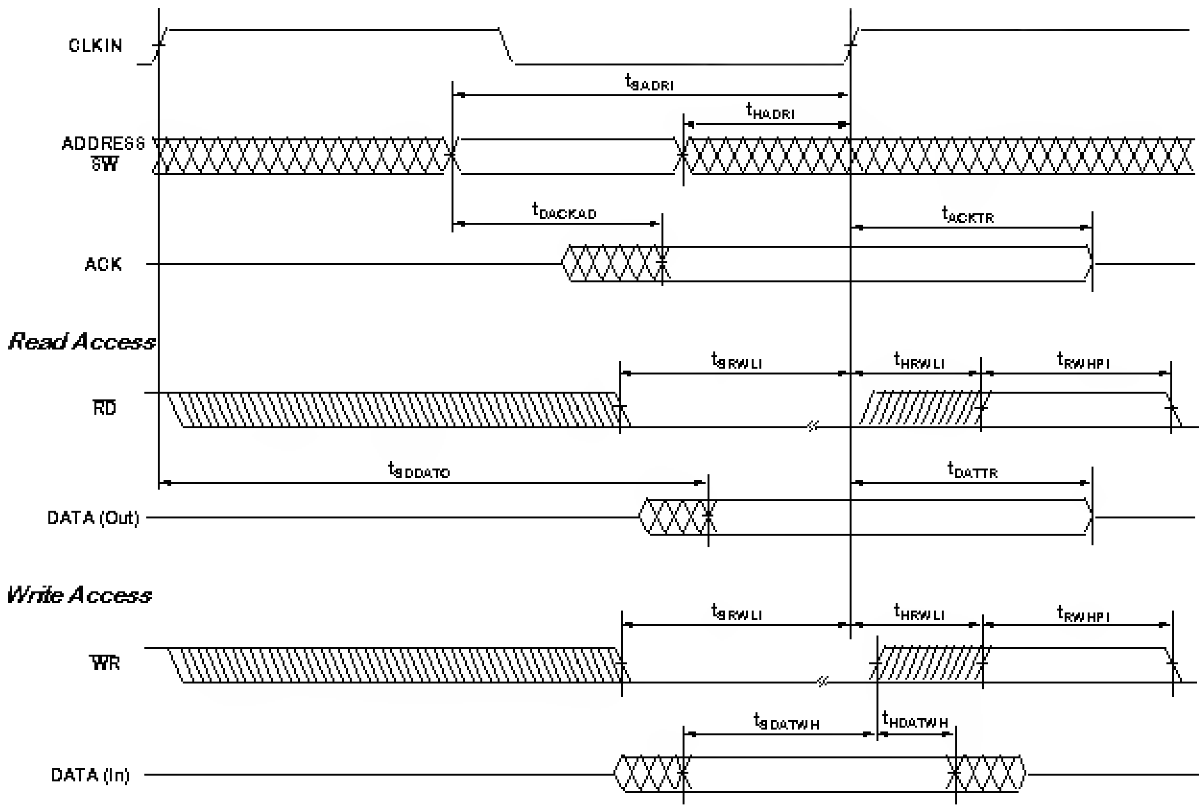


Figure 16 Synchronous Read/Write – Bus Slave

Multiprocessor Bus Request & Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21061Ls ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		Min	Max	Unit
Timing Requirements:				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[3]		20+ 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup before CLKIN[1]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold before CLKIN[1]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold before CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup before CLKIN[4]	13 + DT/2		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold before CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup before CLKIN	20 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold before CLKIN		12 + 3DT/4	ns
Switching Characteristics:				
t_{DHBGO}	$\overline{HBG}$ Delay after CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold after CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BR}$x Delay after CLKIN		5.5 – DT/8	ns
t_{HBRO}	$\overline{BR}$x Hold after CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay after CLKIN		6.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable after CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (o/d) or (a/d) Low from $\overline{CS}$ and $\overline{HBR}$ Low[2]		8.5	ns
t_{TRDYHG}	REDY (o/d) Disable or REDY (a/d) High from $\overline{HBG}$[2]	44 + 27DT/16		ns
t_{ARDYTR}	REDY (a/d) Disable from CS or $\overline{HBR}$ High[2]		10	ns

NOTES

1. Only required for recognition in the current cycle.
2. (o/d)=open drain, (a/d) = active drive.
3. For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR 31-0 must be a non- MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when HBG is asserted. See the "Host Processor Control of the ADSP-2106x" section of the *ADSP-2106x SHARC User's Manual, Second Edition*.
4. $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

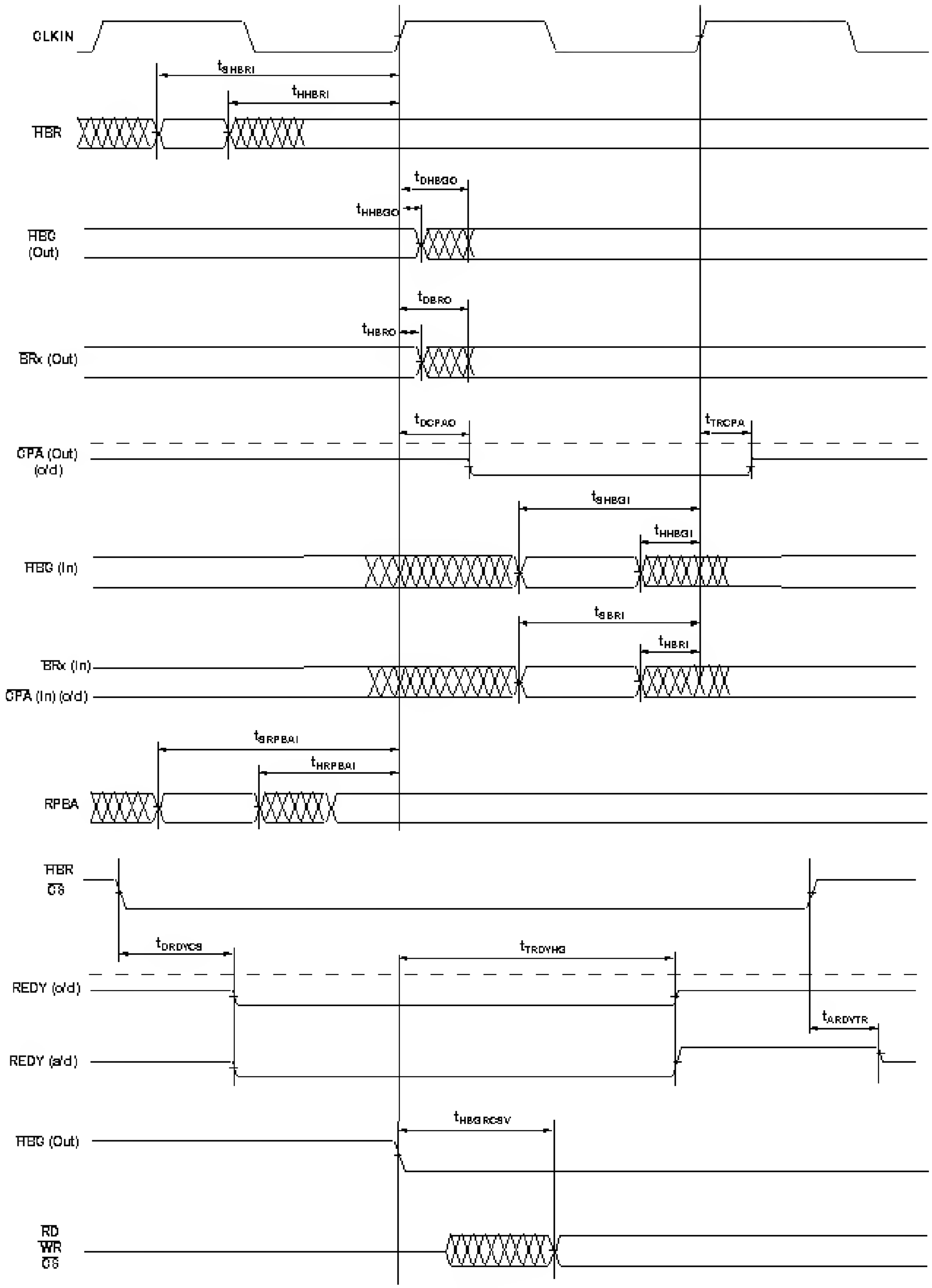


Figure 17 Multiprocessor Bus Request & Host Bus Request

Asynchronous Read/Write – Host to ADSP-21061L

Use these specifications for asynchronous host processor accesses of an ADSP-21061L, after the host has asserted CS and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21061L, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21061L's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Parameter		Min	Max	Unit
Read Cycle				
Timing Requirements:				
t_{SADRDL}	Address Setup/CS low before RD Low[1]	0		ns
t_{HADRDH}	Address Hold/CS hold low after RD	0		ns
t_{WRWH}	RD/WR High Width	6		ns
$t_{DRDHRDY}$	RD High Delay after REDY (o/d) Disable	0		ns
$t_{DRDHRDY}$	RD High Delay after REDY (a/d) Disable	0		ns
Switching Characteristics:				
$t_{SDATRDY}$	Data Valid before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (o/d) or (a/d) Low Delay after RD Low		10	ns
t_{RDYPRD}	REDY (o/d) or (a/d) Low Pulse Width for Read	45 + DT		ns
t_{HDARWH}	Data Disable after RD High	2	8	ns
Write Cycle				
Timing Requirements:				
t_{SCSWRL}	CS low setup before WR low	0		ns
t_{HCSWRH}	CS low hold after WR high	0		ns
t_{SADWRH}	Address Setup before WR High	5		ns
t_{HADWRH}	Address Hold after WR High	2		ns
t_{WWRL}	WR Low Width	7		ns
t_{WRWH}	RD/WR High Width	6		ns
$t_{DWRHRDY}$	WR High Delay after REDY (o/d) or (a/d) Disable	0		ns
t_{SDATWH}	Data Setup before WR High	3		ns
t_{HDATWH}	Data Hold after WR High	1		ns
Switching Characteristics:				
$t_{DRDYWRL}$	REDY (o/d) or (a/d) Low Delay after WR/CS Low		10	ns
t_{RDYPWR}	REDY (o/d) or (a/d) Low Pulse Width for Write	15		ns
t_{SRDYCK}	REDY (o/d) or (a/d) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

NOTES

1. Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR 31-0 must be a non- MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HGB}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the *ADSP-2106x SHARC User's Manual*, *Second Edition*.

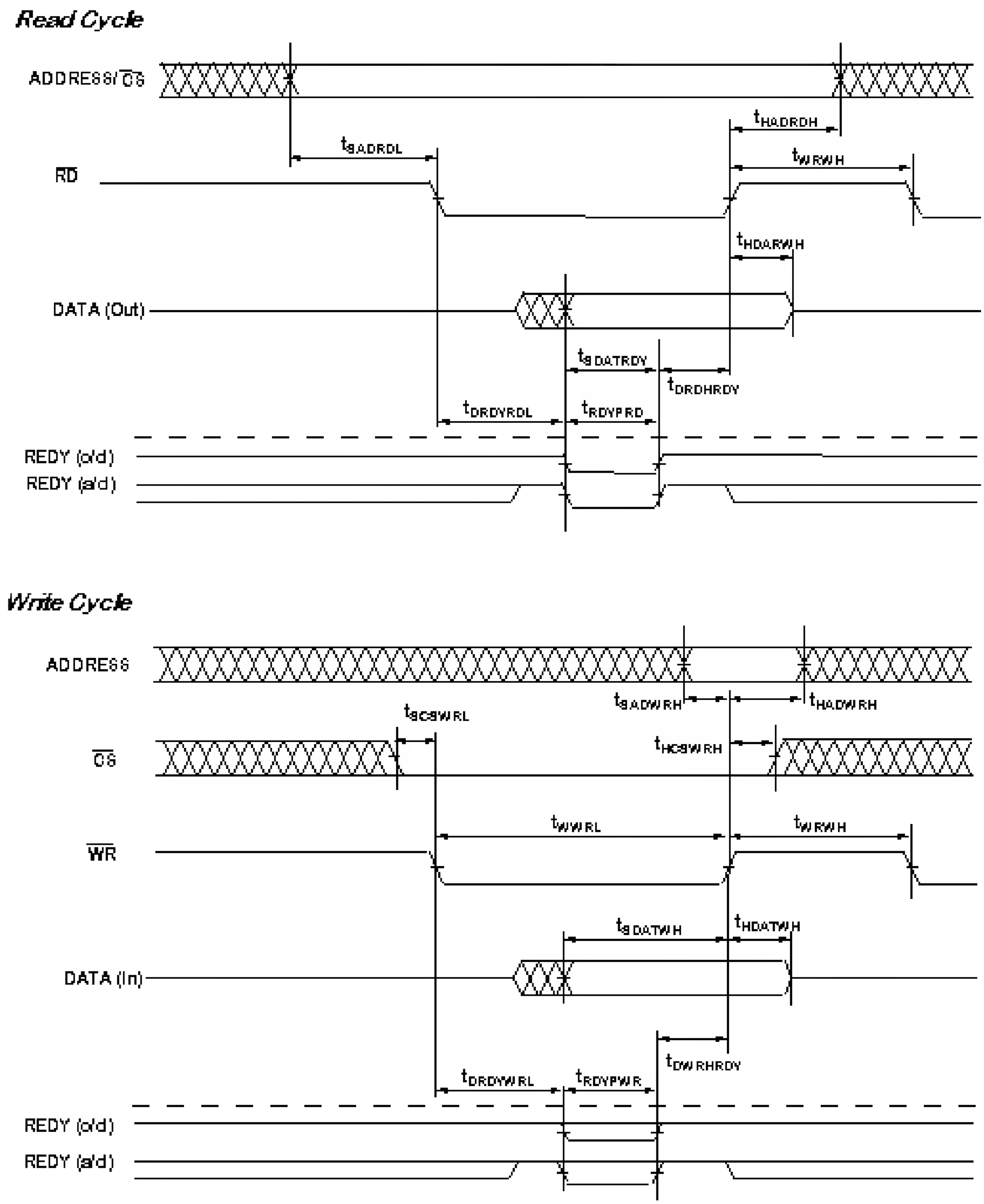


Figure 18 Asynchronous Read/Write - Host to ADSP-21061L

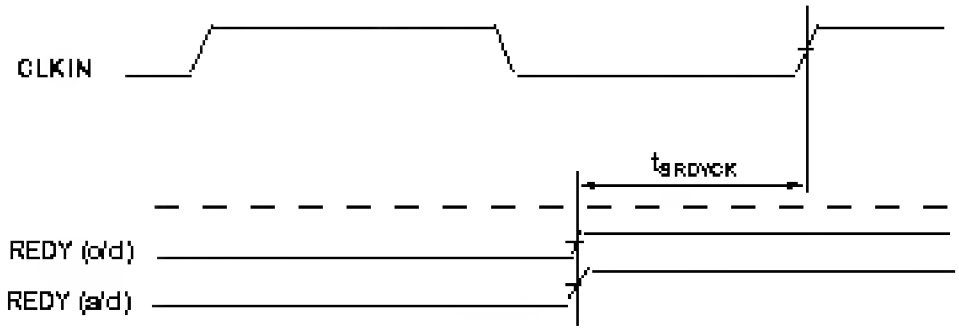


Figure 19 Synchronous REDY Timing

Three-state Timing – Bus Master, Bus Slave, HBR, SBTS

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{SBTS}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{SBTS}$ pin.

Parameter		Min	Max	
Timing Requirements:				
t_{STSCK}	SBTS Setup before CLKIN	12 + DT/2		ns
t_{HTSCK}	SBTS Hold before CLKIN		6 + DT/2	ns
Switching Characteristics:				
t_{MIENA}	Address/Select Enable after CLKIN	–1 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[3]	–1.5 – DT/8		ns
t_{MIENHG}	$\overline{HBG}$ Enable After CLKIN	–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable after CLKIN		0 – DT/4	ns
t_{MITRS}	Strobes Disable after CLKIN[3]		1.5 – DT/4	ns
t_{MITRHG}	$\overline{HBG}$ Disable after CLKIN		2 – DT/4	ns
t_{DATEN}	Data Enable after CLKIN[1]	9 + 5DT/16		ns
t_{DATTR}	Data Disable after CLKIN[1]	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable after CLKIN[I]	7.5 + DT/4		ns
t_{ACKTR}	ACK Disable after CLKIN[I]	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable after CLKIN	–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable after CLKIN		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable before HBG Low[2]	0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable after HBG High[2]	19 + DT		ns

NOTES

1. In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
2. Memory Interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MS}$x, $\overline{SW}$, $\overline{HBG}$, PAGE, $\overline{DMAG}$x, $\overline{BMS}$ (in EPROM boot mode)
3. Strobes = $\overline{RD}$, $\overline{WR}$, $\overline{MS}$x, $\overline{SW}$, PAGE, $\overline{DMAG}$, $\overline{BMS}$

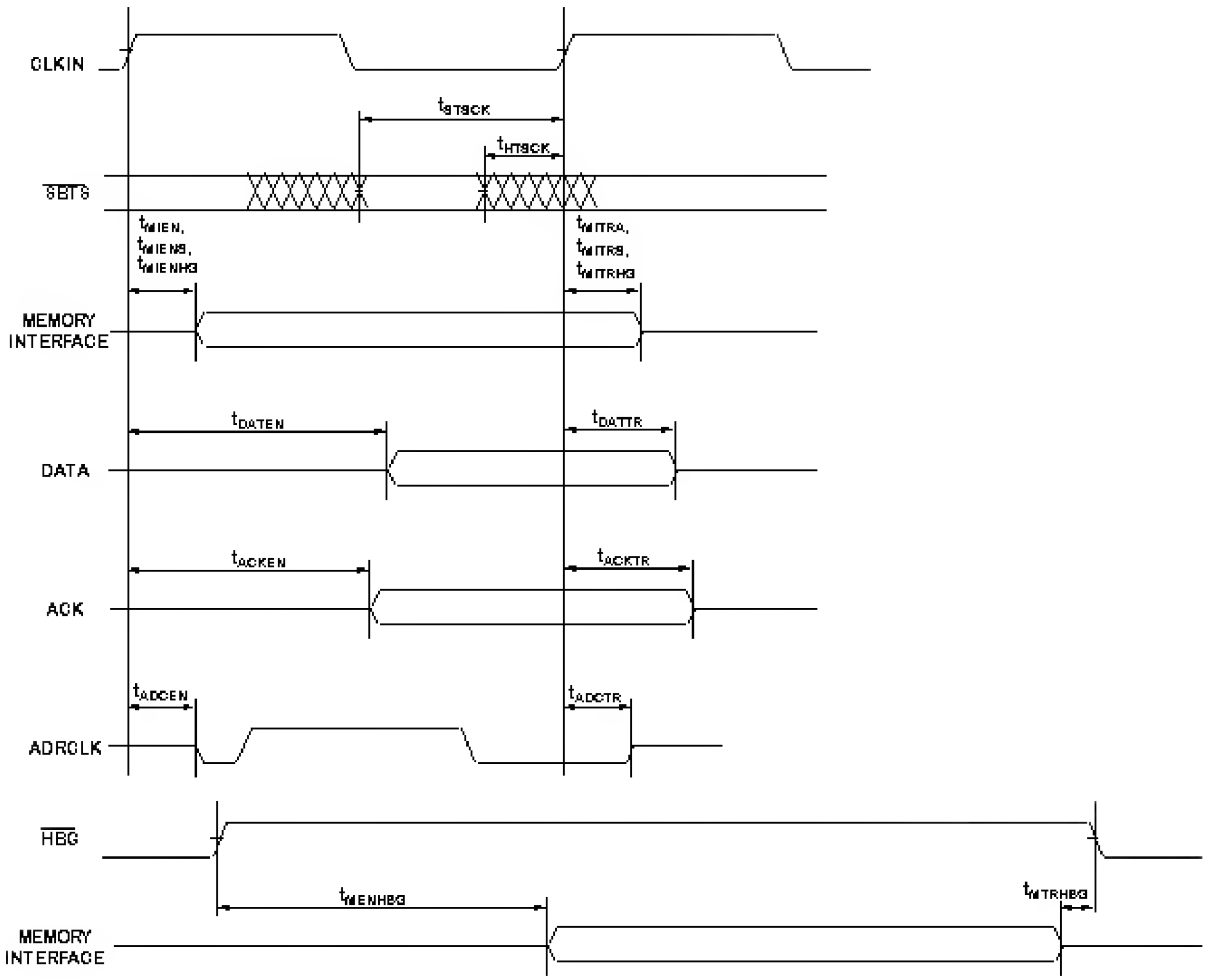


Figure 20 Three-State Timing

Memory interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MS}$x, $\overline{SW}$, $\overline{HBG}$, PAGE, $\overline{DMAG}$x, $\overline{BMS}$, (in EPROM Boot mode)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, $\overline{DMAG}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $ADDR_{31\text{-}0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, PAGE, $\overline{MS}_{3\text{-}0}$, ACK, and $\overline{DMAG}$ signals. For Paced Master mode, the data transfer is controlled by $ADDR_{31\text{-}0}$, RD, WR, $MS_{3\text{-}0}$, and ACK (not $\overline{DMAG}$). For Paced Master mode, the "Memory Read-Bus Master", "Memory Write-Bus Master", and "Synchronous Read/Write-Bus Master timing specifications for $ADDR_{31\text{-}0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3\text{-}0}$, $\overline{SW}$, PAGE, $DATA_{47\text{-}0}$, and ACK also apply.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDRLC}	$\overline{DMAR}$x Low Setup before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{DMAR}$x High Setup before CLKIN[1]	5		ns
t_{WDR}	$\overline{DMAR}$x Width Low (Non-Synchronous)	6		ns
$t_{SDATDGL}$	Data Setup after $\overline{DMAG}$x Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold after $\overline{DMAG}$x High	2		ns
t_{DATDRH}	Data Valid after $\overline{DMAR}$x High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{DMAR}$x Low Edge to Low Edge	23 + 7DT/8		ns
t_{DMARH}	$\overline{DMAR}$x Width High	6		ns
Switching Characteristics:				
t_{DDGL}	$\overline{DMAG}$x Low Delay after CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{DMAG}$x High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{DMAG}$x Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{DMAG}$x High Delay after CLKIN	-2 – DT/8	6 – DT/8	ns
t_{DADGH}	Address Select Valid to $\overline{DMAG}$x High	17 + DT		ns
t_{DDGHA}	Address Select Hold After $\overline{DMAG}$x High	-0.5		ns
$t_{VDATDGH}$	Data Valid before $\overline{DMAG}$x High[3]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable after $\overline{DMAG}$x High[4]	0	7	ns
t_{DGWRL}	$\overline{WR}$ Low before $\overline{DMAG}$x Low	0	2	ns
t_{DGWRH}	$\overline{DMAG}$x Low before $\overline{WR}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{WR}$ High before $\overline{DMAG}$x High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{RD}$ Low before $\overline{DMAG}$x Low	0	2	ns
t_{DRDGH}	$\overline{RD}$ Low before $\overline{DMAG}$x High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{RD}$ High before $\overline{DMAG}$x High	0	3	ns
t_{DGWR}	$\overline{DMAG}$x high to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$ low	5 + 3DT/8 + HI		ns

W = (number of wait states specified in WAIT register) x t_{CK}

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI=0)

NOTES
1. Only required for recognition in the current cycle.
2. $t_{SDATDGL}$ is the data setup requirement if $\overline{DMAR}$x is not being used to hold off completion of a write. Otherwise, if $\overline{DMAR}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMAR}$x is brought high.
3. $t_{VDATDGH}$ is valid if $\overline{DMAR}$x is not being used to hold off completion of a read. If $\overline{DMAR}$x is used to prolong the read, then $t_{VDATDGH} = 8 + 9DT/16 + (n * t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
4. See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and DC loads.

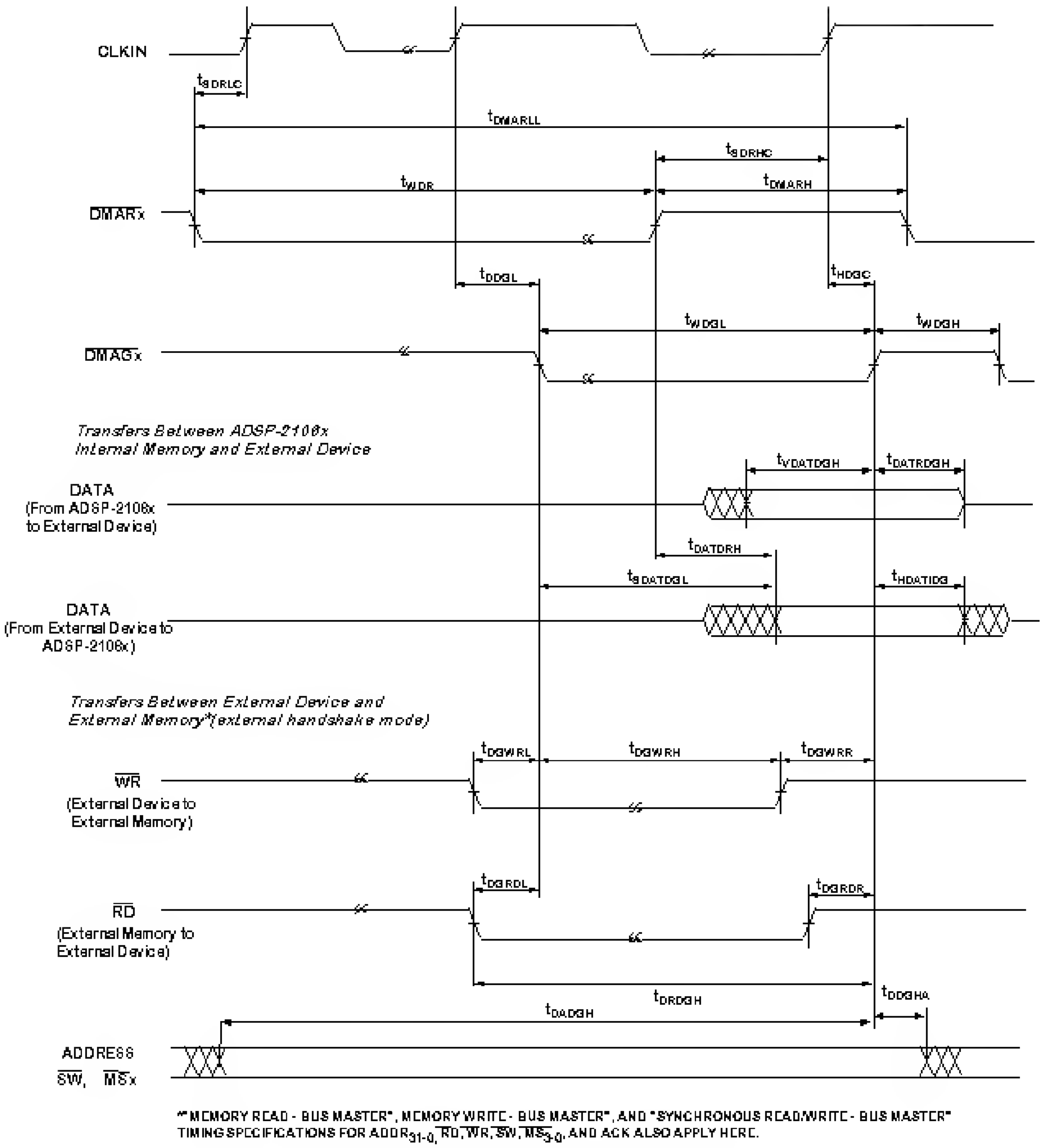


Figure 21 DMA Handshake Timing

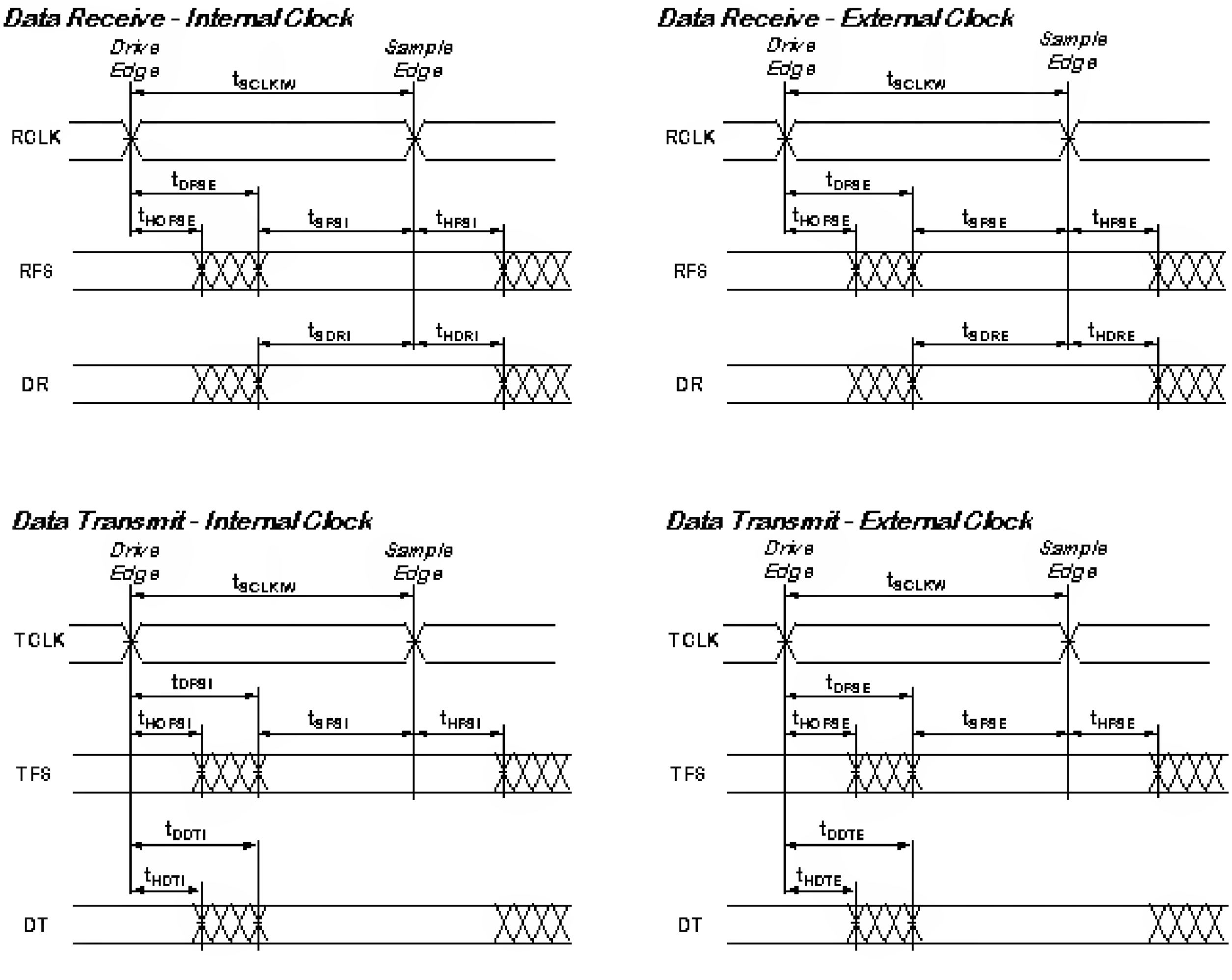
Serial Ports:

Parameter		Min	Max	Unit
External Clock				
Timing Requirements				
t_{SFSE}	TFS/RFS Setup before TCLK/RCLK[2]	3.5		ns
t_{HFSE}	TFS/RFS Hold after TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup before RCLK[2]	1.5		ns
t_{HDRE}	Receive Data Hold after RCLK[2]	4		ns
t_{SCLKW}	TCLK/RCLK Width	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup before TCLK2; RFS Setup before RCLK[2]	8		ns
t_{HFSI}	TFS/RFS Hold after TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup before RCLK[2]	3		ns
t_{HDRI}	Receive Data Hold after RCLK[2]	3		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay after RCLK (Internally Generated RFS)[3]		I3	ns
t_{HOFSE}	RFS Hold after RCLK (Internally Generated RFS)[3]	3		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay after TCLK (Internally Generated TFS)[3]		I3	ns
t_{HOFSE}	TFS Hold after TCLK (Internally Generated TFS)[3]	3		ns
t_{DDTE}	Transmit Data Delay after TCLK[3]		I6	ns
t_{HDTE}	Transmit Data Hold after TCLK[3]	5		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay after TCLK (Internally Generated TFS)[3]		4.5	ns
t_{HOFSI}	TFS Hold after TCLK (Internally Generated TFS)[3]	-I.5		ns
t_{DDTI}	Transmit Data Delay after TCLK[3]		7.5	ns
t_{HDTI}	Transmit Data Hold after TCLK[3]	0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable & Three-state				
Switching Characteristics:				
t_{DDTEN}	Data Enable from External TCLK[3]	4.5		ns
t_{DDTTE}	Data Disable from External RCLK[3]		I0.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[3]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[3]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3DT/8	ns
t_{DPTR}	SPORT Disable after CLKIN		I7	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from late external TFS or external RFS with MCE = I, MFD = 0[4]		I2	ns
$t_{DDTENFS}$	Data Enable from late FS or MCE = 1, MFD = 0[4]	3.5		ns

NOTES:

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay & frame sync setup and hold, 2) data delay & data setup and hold, and 3) SCLK width.

1. RFS hold after RCK when MCE = 1, MFD = 0, is 0 ns minimum from drive edge.
2. Referenced to sample edge.
3. Referenced to drive edge.
4. MCE = I, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$



Note: Either the rising edge or falling edge of RCLK or TCLK can be used as the active sampling edge

Figure 22 Serial Ports

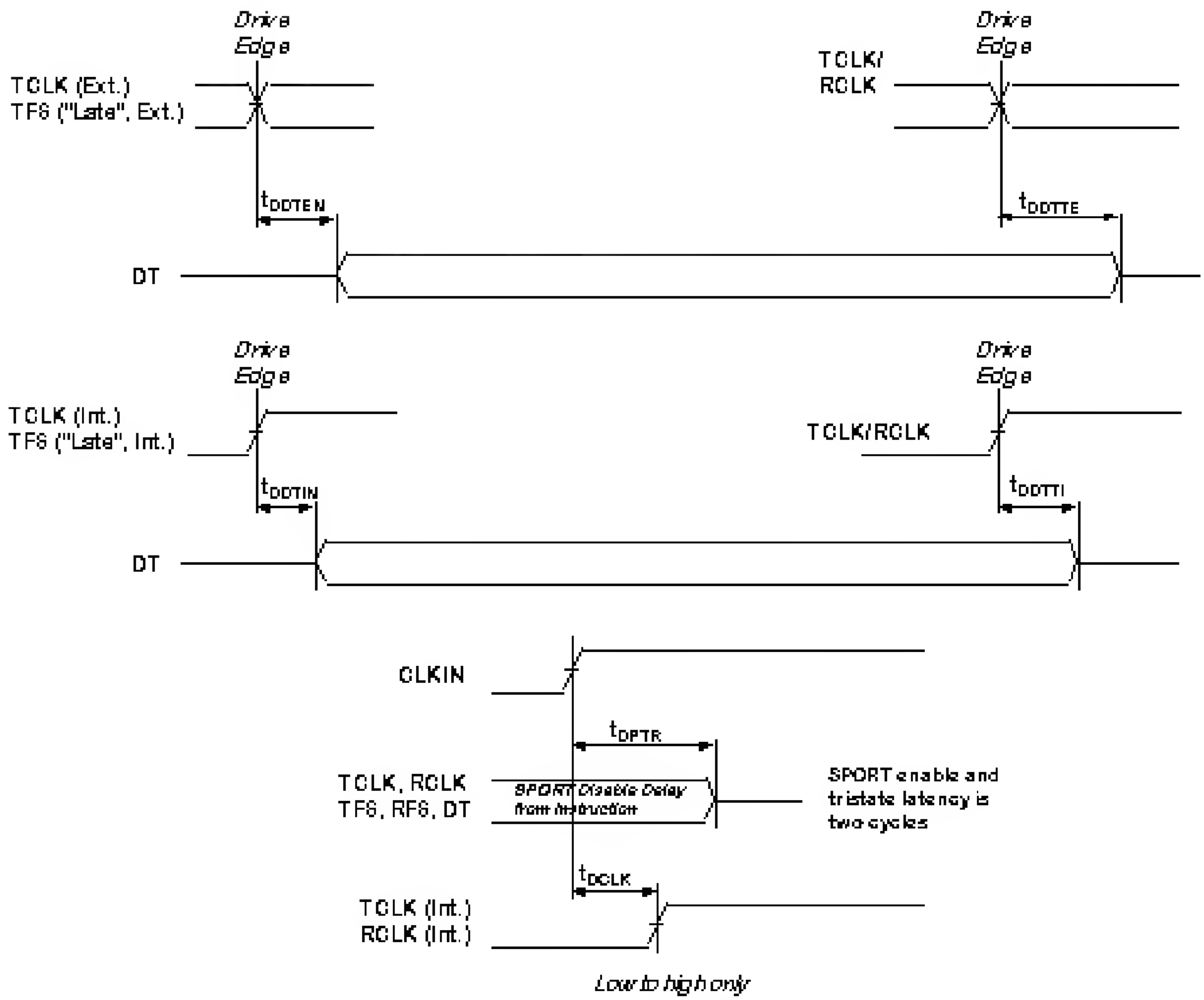


Figure 23 Serial Ports (continued)

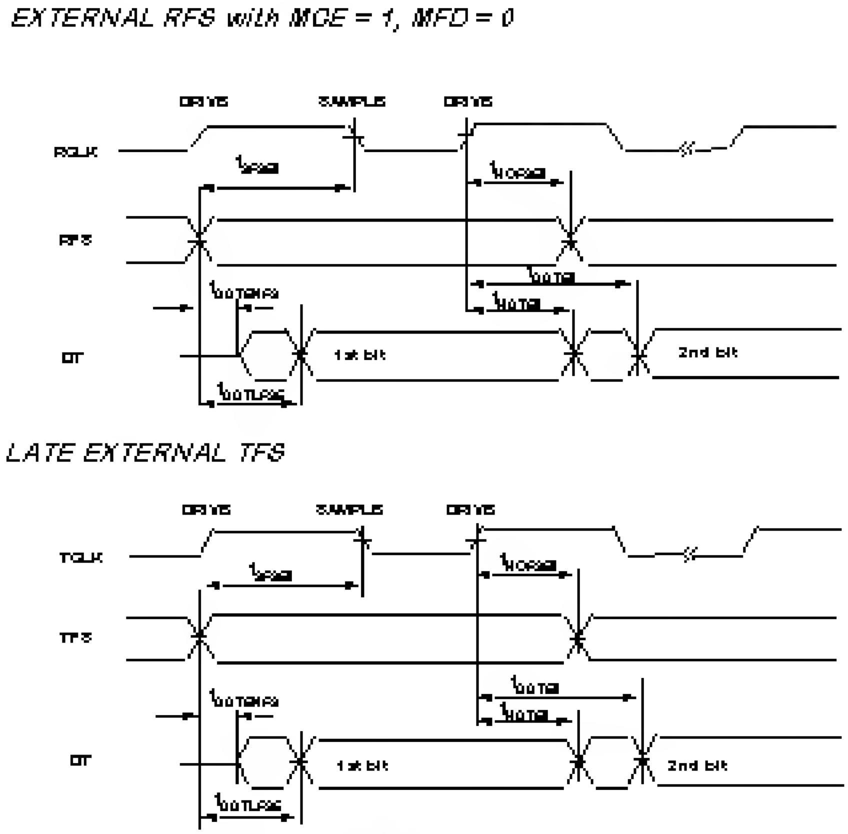


Figure 24 External Late Frame Sync

JTAG Test Access Port & Emulation

Parameter		Min	Max	Unit
Timing Requirements:				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		ns
t_{SSYS}	System Inputs Setup before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold after TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics:				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay after TCK Low[2]		18.5	ns

NOTES

1. System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR}1$, $\overline{DMAR}2$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{IRQ}_{2-0}$, $FLAG_{3-0}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$
2. System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG}1$, $\overline{DMAG}2$, $\overline{BR}_{6-1}$, $\overline{CPA}$, $FLAG_{3-0}$, TIMEXP, DT0, DT1, TCLK0 TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$

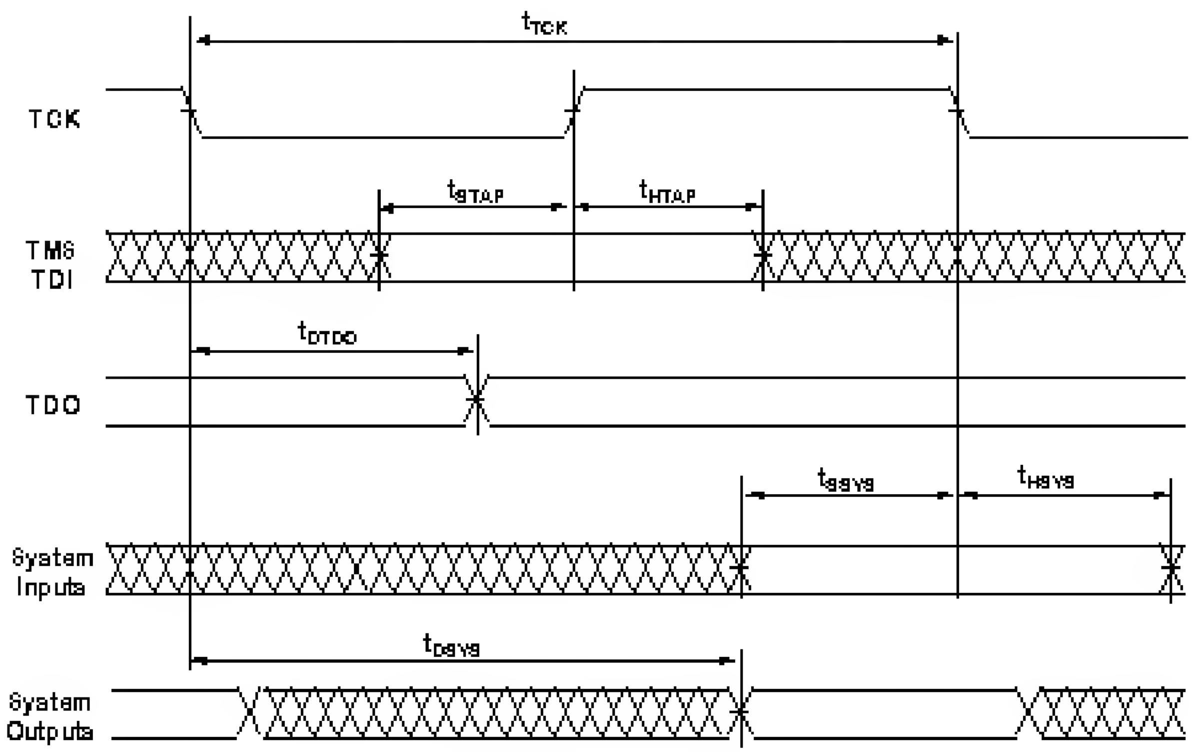


Figure 25 JTAG Test Access Port & Emulation

OUTPUT DRIVE CURRENTS

Figure 26 shows typical I-V characteristics for the output drivers of the ADSP-21061L. The curves represent the current drive capability of the output drivers as a function of output voltage.

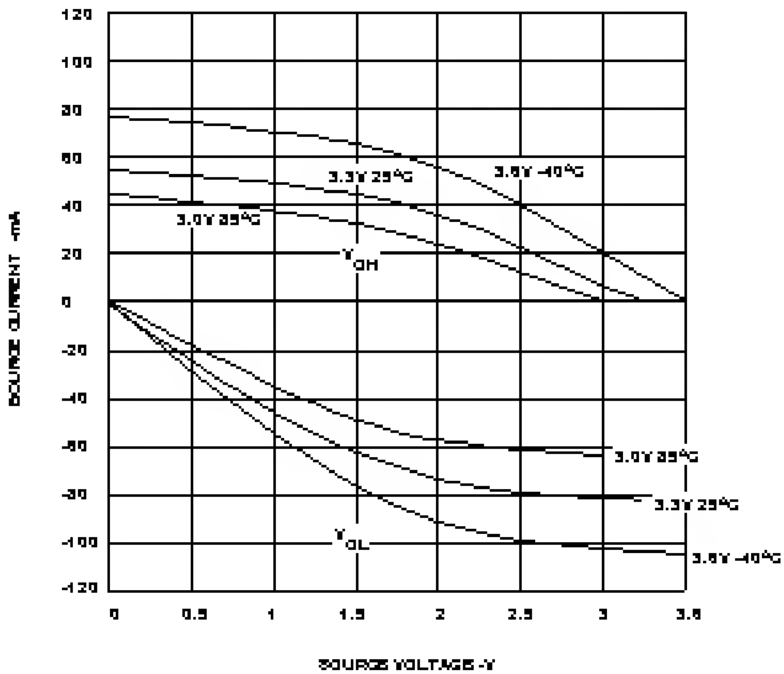


Figure 26 Typical Drive Currents

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$PINT = I_{DDIN2} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

For example:

Estimate P_{EXT} with the following assumptions:

- a system with one bank of external data memory RAM (32-bit)
- four 128K x 8 RAM chips are used, each with a load of 10 pF
- external data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with
- 50% of the pins switching
- the instruction cycle rate is 40 MHz (t_{CK} = 25 ns) and V_{DD} = 3.3V

The P_{EXT} equation is calculated for each class of pins that can drive:

Pin Type	# of Pins	% Switching	xC	xf	xV_{DD}^2	$=P_{EXT}$
Address	15	50%	x 44.7 pF	x 20 MHz	x 10.9 V	**=0.072 W**
$\overline{MS0}$	1	0%	x 44.7 pF	x 20 MHz	x 10.9 V	**=0.000 W**
$\overline{WR}$	1	–	x 44.7 pF	x 40 MHz	x 10.9 V	**=0.019 W**
Data	32	50%	x 14.7 pF	x 20 MHz	x 10.9 V	**=0.051 W**
ADRCLK	1	–	x 4.7 pF	x 40 MHz	x 10.9 V	**=0.002 W**

P_{EXT} = 0.144 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \text{ x } 3.3 \text{ V})$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{IN}T. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Also note that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_{L} \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 25. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21061L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e. t_{DATRWH} for the write cycle).

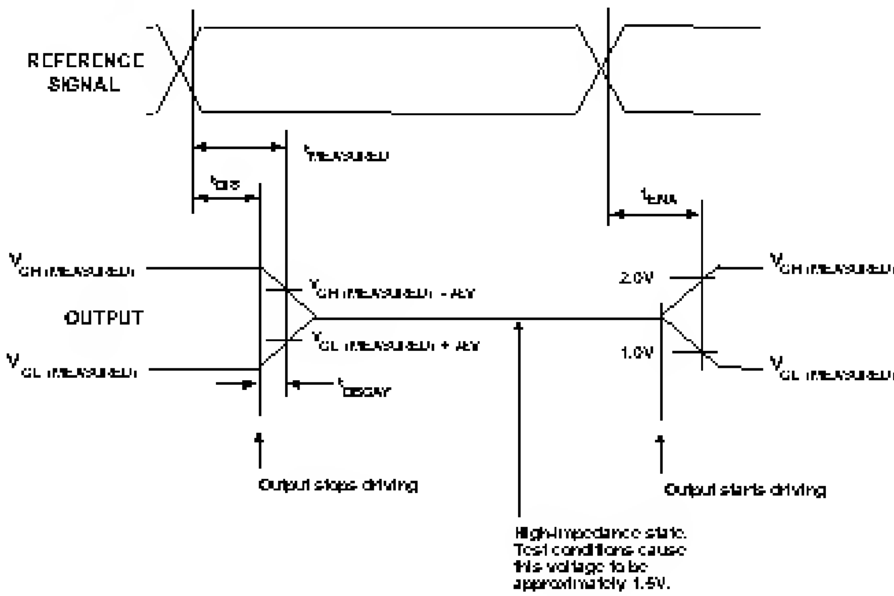


Figure 27 Output Enable

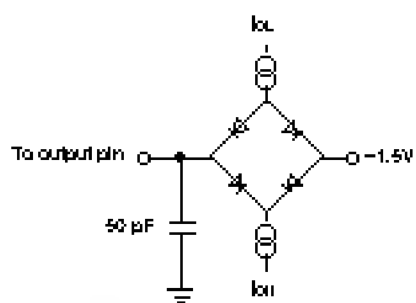


Figure 28 Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 29 Voltage Reference Levels for AC Measurements (Except Output Enable/Disable

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of 1.5ns/50pF for loads other than the nominal value of 50 pF. Figure 30 shows how output rise time varies with capacitance. Figure 32 shows graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section "Output Disable Time" under "Test Conditions.") The graphs of Figures 30, 31, and 32 may not be linear outside the ranges shown.

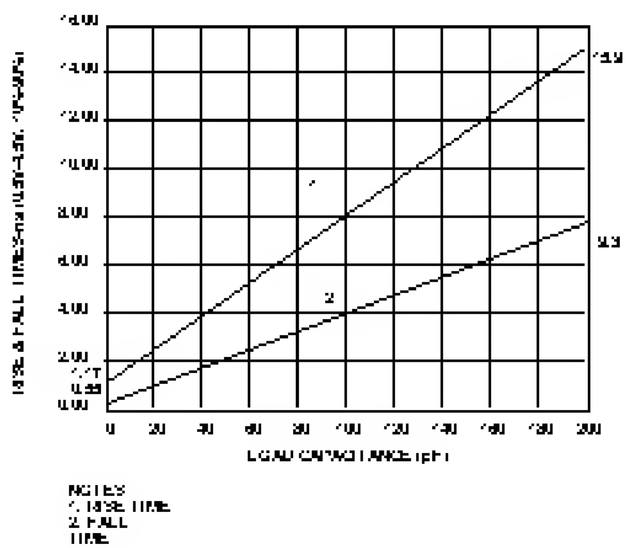


Figure 30 Typical Rise Time (10%-90% V_{DD}) vs. Load Capacitance

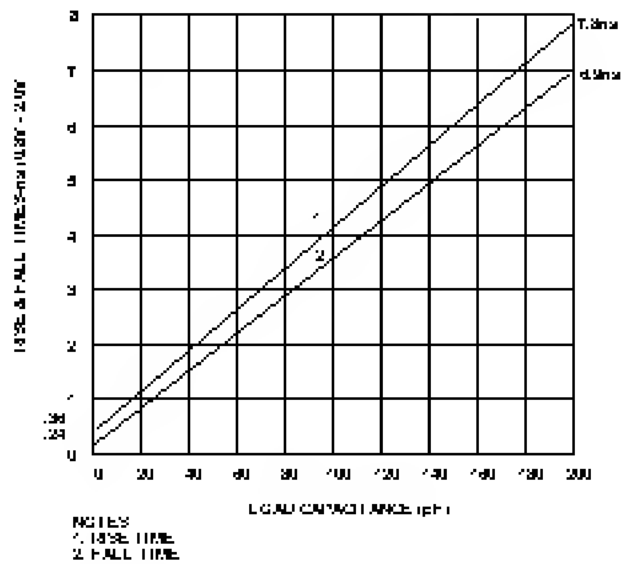


Figure 31 Typical Output Rise Time (0.8V–2.0V) vs. Load Capacitance

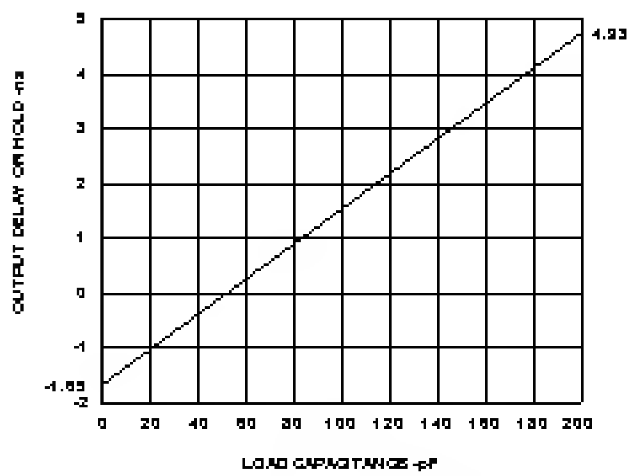


Figure 32 Typical Output Delay or Hold vs. Load Capacitance

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061L is packaged in a 240-lead thermally enhanced PQFP. The top surface of the package contains a copper slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the copper slug is internally connected to GND through the device substrate.

The ADSP-21061L is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, a heat sink and/or an air flow source may be used. A heat sink should be attached with a thermal adhesive.

$T_{CASE} = T_{AMB} + (PD \times \Theta CA)$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under "Power Dissipation")

$\Theta JC = 0.3\ ° C/W$

Air flow

(Linear Ft./Min.)	0	100	200	400	600
ΘCA (° C/W)	26	22.5	21	19	17

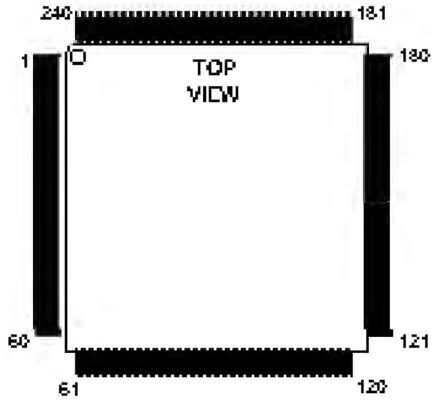
Notes:

This represents preliminary thermal resistance at total power of 1.5W.

With air flow, no variance is seen in θCA with power.

θCA at 0 LFM varies with power: At 2W, θCA = TBD° C/W, at 3W θCA = TBD° C/W.

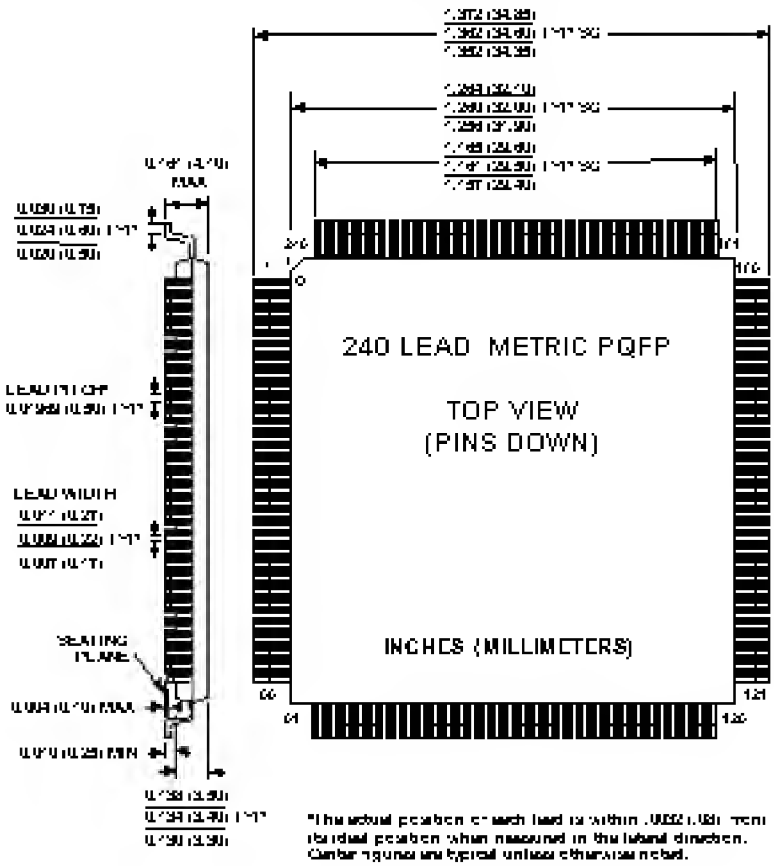
ADSP-21061L 240-LEAD PQFP PACKAGE PINOUT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TDI	41	ADDR20	81	TCLK0	121	DATA41	161	DATA14	201	NC
2	$\overline{TRST}$	42	ADDR21	82	TFS0	122	DATA40	162	DATA13	202	NC
3	VDD	43	GND	83	DR0	123	DATA39	163	DATA12	203	NC
4	TDO	44	ADDR22	84	RCLK0	124	VDD	164	GND	204	NC
5	TIMEXP	45	ADDR23	85	RFS0	125	DATA38	165	DATA11	205	VDD
6	$\overline{EMU}$	46	ADDR24	86	VDD	126	DATA37	166	DATA10	206	NC
7	ICSA	47	VDD	87	VDD	127	DATA36	167	DATA9	207	NC
8	FLAG3	48	GND	88	GND	128	GND	168	VDD	208	NC
9	FLAG2	49	VDD	89	ADRCLK	129	NC	169	DATA8	209	NC
10	FLAG1	50	ADDR25	90	REDY	130	DATA35	170	DATA7	210	NC
11	FLAG0	51	ADDR26	91	$\overline{HBG}$	131	DATA34	171	DATA6	211	NC
12	GND	52	ADDR27	92	$\overline{CS}$	132	DATA33	172	GND	212	GND
13	ADDR0	53	EGND	93	$\overline{RD}$	133	VDD	173	DATA5	213	NC
14	ADDR1	54	$\overline{MS3}$	94	$\overline{WR}$	134	VDD	174	DATA4	214	NC
15	VDD	55	$\overline{MS2}$	95	GND	135	GND	175	DATA3	215	NC
16	ADDR2	56	$\overline{MS1}$	96	VDD	136	DATA32	176	VDD	216	NC
17	ADDR3	57	$\overline{MS0}$	97	GND	137	DATA31	177	DATA2	217	NC
18	ADDR4	58	$\overline{SW}$	98	CLKIN	138	DATA30	178	DATA1	218	NC
19	GND	59	$\overline{BMS}$	99	ACK	139	GND	179	DATA0	219	VDD
20	ADDR5	60	ADDR28	100	$\overline{DMAG2}$	140	DATA29	180	GND	220	GND
21	ADDR6	61	GND	101	$\overline{DMAG1}$	141	DATA28	181	GND	221	VDD
22	ADDR7	62	VDD	102	PAGE	142	DATA27	182	NC	222	NC
23	VDD	63	VDD	103	VDD	143	VDD	183	NC	223	NC
24	ADDR8	64	ADDR29	104	$\overline{BR6}$	144	VDD	184	NC	224	NC
25	ADDR9	65	ADDR30	105	$\overline{BR5}$	145	DATA26	185	NC	225	NC
26	ADDR10	66	ADDR31	106	$\overline{BR4}$	146	DATA25	186	NC	226	NC
27	GND	67	GND	107	$\overline{BR3}$	147	DATA24	187	NC	227	NC
28	ADDR11	68	$\overline{SBTS}$	108	$\overline{BR2}$	148	GND	188	VDD	228	GND
29	ADDR12	69	$\overline{DMAR2}$	109	$\overline{BR1}$	149	DATA23	189	NC	229	ID2
30	ADDR13	70	$\overline{DMAR1}$	110	GND	150	DATA22	190	NC	230	ID1
31	VDD	71	$\overline{HBR}$	111	VDD	151	DATA21	191	NC	231	ID0
32	ADDR14	72	DT1	112	GND	152	VDD	192	NC	232	LBOOT
33	ADDR15	73	TCLK1	113	DATA47	153	DATA20	193	NC	233	RPBA
34	GND	74	TFS1	114	DATA46	154	DATA19	194	NC	234	$\overline{RESET}$
35	ADDR16	75	DR1	115	DATA45	155	DATA18	195	GND	235	EBOOT
36	ADDR17	76	RCLK1	116	VDD	156	GND	196	GND	236	$\overline{IRQ2}$
37	ADDR18	77	RFS1	117	DATA44	157	DATA17	197	VDD	237	$\overline{IRQ1}$
38	VDD	78	GND	118	DATA43	158	DATA16	198	NC	238	$\overline{IRQ0}$
39	VDD	79	$\overline{CPA}$	119	DATA42	159	DATA15	199	NC	239	TCK
40	ADDR19	80	DT0	120	GND	160	VDD	200	NC	240	TMS

PACKAGE OUTLINE DIMENSIONS

240-Lead Metric PQFP



Ordering Guide

Part Number	Case Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage
ADSP-21061LKS-133x	0°C – 85°C	33 MHz	1Mbit	3.3V
ADSP-21061LKS-160x	0°C – 85°C	40 MHz	1Mbit	3.3V

Printed In USA

P3200-2.5-9/97